VERIFICATION OF TRANSLATION

I, Kyozo Omori, translator of 1699-7, Ochibara, Sanda, Hyogo, Japan, hereby declare that I am conversant with the English and Japanese languages and am a competent translator thereof. I further declare that to the best of my knowledge and belief the following is a true and correct translation made by me of Japanese Patent Application No. 2004-026851 filed on February 3, 2004.

Date: January 25, 2008

Kyozo Omori

KYOZO OMORI

[DOCUMENT] Patent Application

[OUR REFERENCE NO.] 2925150076

[FILING DATE OF APPLICATION] February 3, 2004

[To] Commissioner, Patent Office

[INTERNATIONAL PATENT CLASSIFICATION] H01L 33/00

[INVENTOR]

[ADDRESS] c/o Matsushita Electric Industrial Co., Ltd.
1006, Kadoma, Kadoma-City, Osaka

[NAME] Hideo Nagai

[APPLICANT]

[CODE NO.] 000005821

[NAME] Matsushita Electric Industrial Co., Ltd.

[PATENT AGENT]

[CODE NO.] 100090446

[PATENT ATTORNEY]

[NAME] Shiro NAKAJIMA

[CHARGES]

[RECEIPT NO.] 014823

[AMOUNT] ¥21,000

[LIST OF ENCLOSURES]

Claims	1
Specification	1
Drawings	1
Abstract	1

[POWER OF ATTORNEY NO.] 9003742

[DOCUMENT] Claims

[CLAIM 1] A semiconductor light emitting device to be implemented, comprising:

a multilayer epitaxial structure including a light emitting layer; and

a base substrate whose main surfaces are slightly larger than main surfaces of the multilayer epitaxial structure, wherein

the multilayer epitaxial structure is formed on one of the main surfaces of the base substrate with a space being retained along a periphery of the base substrate, and a phosphor film covers side surfaces and a main surface of the multilayer epitaxial structure which is opposite to the main surface to which the base substrate is connected.

[CLAIM 2] The semiconductor light emitting device of Claim 1, wherein

the multilayer epitaxial structure is first epitaxially grown on a single-crystal substrate, and then transferred to the base substrate.

[CLAIM 3] The semiconductor light emitting device of Claim 1 or Claim 2, further comprising:

a metal reflective film that is sandwiched between the multilayer epitaxial structure and the base substrate.

[CLAIM 4] The semiconductor light emitting device of one of Claims 1 through 3, wherein

the multilayer epitaxial structure includes a p-type semiconductor layer and an n-type semiconductor layer that are stacked in above-stated order from a base substrate side.

[CLAIM 5] The semiconductor light emitting device of Claim 4, wherein

a main surface of the n-type semiconductor layer which faces away from the light emitting layer is uneven so as to improve light extraction efficiency.

[CLAIM 6] A lighting module comprising:

a printed-wiring board; and

a semiconductor light emitting device that is claimed in one of Claims 1 through 5, and is mounted on the printed-wiring board.

[CLAIM 7] A lighting apparatus including, as a light source, the lighting module claimed in Claim 6.

[CLAIM 8] A display element including, as a light source, a semiconductor light emitting device claimed in one of Claims 1 through 5.

[CLAIM 9] A manufacturing method of a semiconductor light emitting device, comprising the steps of:

forming a multilayer epitaxial structure including a light emitting layer on a main surface of a base substrate by epitaxial growth;

forming a first metal film on an outmost layer of the multilayer epitaxial structure;

forming a second metal film on a base substrate;

adhering the single-crystal substrate to the base substrate in such a manner that the first metal film is connected to the second metal film;

separating the single-crystal substrate from the multilayer epitaxial structure;

dividing the multilayer epitaxial structure into a plurality

of portions each of which is the semiconductor light emitting device, prior to the adhering step or subsequent to the separating step;

forming a phosphor film that covers all exposed surfaces of each of the plurality of portions, subsequent to the separating step and the dividing step; and

dicing the base substrate according to each of the plurality of portions.

[DOCUMENT] Specification

[TITLE OF THE INVENTION] SEMICONDUCTOR LIGHT EMITTING DEVICE, LIGHTING MODULE, LIGHTING APPARATUS, DISPLAY ELEMENT AND MANUFACTURING METHOD OF SEMICONDUCTOR LIGHT EMITTING DEVICE

[FIELD OF THE INVENTION]

0001

The present invention relates to a semiconductor light emitting device such as a light emitting diode chip (LED chip), and also to a light emitting module, a lighting apparatus and a display element using the semiconductor light emitting device, and a manufacturing method of the semiconductor light emitting device. The present invention particularly relates to a semiconductor light emitting device that emits light of a desired color using a phosphor.

[DESCRIPTION OF THE RELATED ART]

0002

LEDs have a higher efficiency and a longer lifetime than incandescent lamps and halogen lamps. In the field of LEDs, vigorous researches have recently been conducted to use white LEDs for lighting, as white LEDs with higher luminance have been developed. A common white LED at present includes a combination of an LED bare chip emitting blue light and a phosphor excited by the blue light to emit yellow light, so that the blue light and the yellow light mix together to generate white light.

0003

A manufacturing method of this white LED includes a wafer fabrication process in which the LED bare chip is obtained and an assembly process in which the LED bare chip is packaged.

In the wafer fabrication process, the LED bare chip is typically obtained by forming a multilayer epitaxial structure including a light emitting layer on a light-transmitting substrate, such as a sapphire

substrate by epitaxial growth. In addition, an anode electrode and a cathode electrode are formed on a main surface of the multilayer epitaxial structure which faces away from the sapphire substrate.

0004

In the assembly process, the LED bare chip is mounted on a lead frame, a printed-wiring board or the like since the LED bare chip alone can not be put to use. After this, a resin mixed with a phosphor material is dropped onto the mounted LED bare chip and cured, to form a phosphor film. Subsequently, steps such as molding a periphery of the phosphor film using a resin are conducted to complete the white LED. The completed white LED is tested for its electrical and optical performance before shipped.

0005

However, there is a high possibility that the white LED manufactured in the above-descried manner has poor optical performance. The reason is explained in the following. Firstly, the phosphor film is formed in such a manner that the resin mixed with the phosphor material is dropped onto the LED bare chip and then cured. Therefore, it is highly likely that the thickness of the phosphor film in the white LED is not equal to a designed thickness. Here, a color temperature of the white light emitted by the white LED is determined by a ratio between a quantity of the blue light and a quantity of the yellow light. This being so, if the phosphor film is thick, the quantity of the blue light is small and the quantity of the yellow light is large, so that white light of a low color temperature is produced. On the other hand, if the phosphor film is thin, white light of a high color temperature is produced. Consequently, a desired color temperature can not be realized. Secondly, the phosphor film tends to be formed at an uneven thickness. If the phosphor film is formed at an inappropriately uneven thickness, unevenness of color occurs.

0006

White LEDs with the above-mentioned defects are rejected as a result of the optical performance test. This results in a low ratio of accepted finished products (white LEDs) to all finished products.

In an attempt to improve the ratio of accepted finished products, it has been proposed to test white LEDs for unevenness of color prior to the assembly process. This proposal has been realized by an LED chip that is disclosed in Patent Document 1.

0007

According to this disclosure, an LED bare chip is mounted on a substrate (an auxiliary mounting substrate) that has a slightly larger surface area than the LED bare chip, with a multilayer epitaxial structure facing downwards (i.e. a sapphire substrate of the LED bare chip faces upwards). A phosphor film is then formed on and around the LED bare chip mounted on the auxiliary mounting substrate. Thus, this LED bare chip can be tested for its optical performance prior to an assembly process in which the LED bare chip is mounted on a lead frame or a printed-wiring board. As a consequence, the ratio of accepted finished products can be improved.

[Patent Document 1] Japanese patent Application Publication No. 2001-15817 (Japanese patent No. 3399440)

[DISCLOSURE OF THE INVENTION]

[THE PROBLEMS THE INVENTION IS GOING TO SOLVE]

0008

However, the LED chip disclosed in Patent Document 1 has an extra constituent, i.e. the auxiliary mounting substrate. Accordingly, an entire thickness (height) of the LED chip increases by a thickness of the auxiliary mounting substrate, which results in an increase in chip size.

In light of the above-described problems, an object of the present invention is to provide a semiconductor light emitting device which can be tested for its optical performance before packaged without increasing a size of the semiconductor light emitting device. The object includes provision of a manufacturing method of the semiconductor light emitting device, and a lighting module, a lighting apparatus and a display element using the semiconductor light emitting device.

[MEANS TO SOLVE THE PROBLEMS]

0009

One aspect of the present invention for solving the above-described problems is provided as a semiconductor light emitting device to be implemented, comprising: a multilayer epitaxial structure including a light emitting layer; and a base substrate whose main surfaces are slightly larger than main surfaces of the multilayer epitaxial structure, wherein the multilayer epitaxial structure is formed on one of the main surfaces of the base substrate with a space being retained along a periphery of the base substrate, and a phosphor film covers side surfaces and a main surface of the multilayer epitaxial structure which is opposite to the main surface to which the base substrate is connected.

0010

In the above-described semiconductor light emitting device, the multilayer epitaxial structure may be first epitaxially grown on a single-crystal substrate, and then transferred to the base substrate.

The above-described semiconductor light emitting device may further comprise: a metal reflective film that is sandwiched between the multilayer epitaxial structure and the base substrate.

In the above-described semiconductor light emitting device, the

multilayer epitaxial structure may include a p-type semiconductor layer and an n-type semiconductor layer that are stacked in above-stated order from a base substrate side.

0011

In the above-described semiconductor light emitting device, a main surface of the n-type semiconductor layer which faces away from the light emitting layer may be uneven so as to improve light extraction efficiency.

Another aspect of the present invention for solving the above-described problems is provided as a lighting module comprising: a printed-wiring board; and one of the above-described semiconductor light emitting devices, mounted on the printed-wiring board.

Still another aspect of the present invention for solving the above-described problems is provided as a lighting apparatus including, as a light source, the above-described lighting module.

0012

Yet another aspect of the present invention for solving the above-described problems is provided as a display element including, as a light source, one of the above-described.

Yet still another aspect of the present invention for solving the above-described problems is provided as a manufacturing method of a semiconductor light emitting device, comprising the steps of: forming a multilayer epitaxial structure including a light emitting layer on a main surface of a base substrate by epitaxial growth; forming a first metal film on an outmost layer of the multilayer epitaxial structure; forming a second metal film on a base substrate; adhering the single-crystal substrate to the base substrate in such a manner that the first metal film is connected to the second metal film; separating the single-crystal substrate from the multilayer epitaxial structure; dividing the multilayer epitaxial structure into a

plurality of portions each of which is the semiconductor light emitting device, prior to the adhering step or subsequent to the separating step; forming a phosphor film that covers all exposed surfaces of each of the plurality of portions, subsequent to the separating step and the dividing step; and dicing the base substrate according to each of the plurality of portions.

[EFFECTS OF THE INVENTION]

0013

According to the semiconductor light emitting device, being one aspect of the present invention, the main surfaces of the base substrate are slightly larger than the main surfaces of the multilayer epitaxial structure, and the multilayer epitaxial structure is formed on one of the main surfaces of the base substrate with a space being retained along a periphery of the base substrate, and a phosphor film covers side surfaces and a main surface of the multilayer epitaxial structure which is opposite to the main surface to which the base substrate is connected. The semiconductor light emitting device with this structure can be tested for its optical performance, such as unevenness of color, before mounted. That is to say, the semiconductor light emitting device can be tested before it is mounted on a lead frame or a printed-wiring board. Accordingly, a ratio of accepted finished products to all finished products can be improved. Moreover, since an additional member such as an auxiliary mounting substrate is not required as in conventional technologies, the semiconductor light emitting device is not increased in size.

0014

The lighting module or the lighting apparatus, being other aspects of the present invention, includes the above-described semiconductor light emitting device. Accordingly, for the same

reasons stated above, the ratio of accepted finished product (the lighting module or the lighting apparatus) can be improved, and the cost can be reduced.

The manufacturing method of the semiconductor light emitting device, being another aspect of the present invention, enables the semiconductor light emitting device, which produces the above-described effects, to be manufactured.

[BEST MODE FOR CARRYING OUT THE INVENTION]

0015

In the following, several embodiments of the present invention will be described with reference to the attached drawings.

<First Embodiment>

Fig. 1A is a plan view illustrating a white LED chip 2 which is one type of a semiconductor light emitting device (hereinafter simply referred to as "an LED chip 2"), Fig. 1B illustrates a cross-section of the LED chip 2 along a line AA shown in Fig. 1A, and Fig. 1C is a bottom plan view illustrating the LED chip 2. Here, Fig. 1A illustrates the LED chip 2 after removing a phosphor film 8 (shown in Fig. 1B and mentioned later). It should be noted that a reduced scale for each constituent is not uniform in any of the drawings including Figs. 1A, 1B and 1C.

0016

As shown in Fig. 1B, the LED chip 2 is formed in such a manner that a multilayer epitaxial structure 6 and the phosphor film 8 are formed on a high-resistive Si substrate 4 which is a base substrate (hereinafter referred to as "an Si substrate 4"). A main surface of the Si substrate 4 is slightly larger than a main surface of the multilayer epitaxial structure 6. The multilayer epitaxial structure 6 is formed on one of the main surfaces of the Si substrate 4 with

a space being retained along a periphery of the substrate 4.

The multilayer epitaxial structure 6 is made up of a p-AlGaN layer 10 which is a conductive layer (having a thickness of 200 nm), a InGaN/AlGaN MQW light emitting layer 12 (having a thickness of 40 nm), and an n-AlGaN layer 14 which is a conductive layer (having a thickness of 2 μm). The layer 10 is the closest to the Si Substrate 4, and then the layers 12 and 14 are formed in the stated order. The multilayer epitaxial structure 6 has a diode structure.

0017

The LED chip 2 is a 500-μm-square and has a thickness of 300 μm (the Si substrate 4 has a thickness of 100 μm, and the phosphor film 8 has a thickness of 200 μm with respect to an upper main surface of the Si substrate 4). The multilayer epitaxial structure 6 has the above-mentioned thickness and is a 420-μm-square.

A high-reflective Rh/Pt/Au electrode 16 is formed on the entire lower main surface of the p-AlGaN layer 10, which is opposite to a main surface on which the light emitting layer 12 is formed. It should be noted that the multilayer epitaxial structure 6 and the high-reflective electrode 16 are first formed on a different sapphire substrate 42 (shown in Fig. 2 and mentioned later) using a wafer fabrication process, and then transferred to the Si substrate 4.

0018

A conductive film 18 which is made of a conductive material is formed, at least, in an area corresponding to the high-reflective electrode 16 on an upper main surface of the Si substrate 4. The conductive film 18 is made of Ti/Pt/Au, and connected to the high-reflective electrode 16 by a connection layer 20 which is made of a conductive material such as Au/Sn.

A light extraction surface of the multilayer epitaxial structure 6 is an upper main surface of the n-AlGaN layer 14, which is opposite

to a main surface to which the light emitting layer 12 is connected. Here, depressions 22 are formed on the upper main surface of the layer 14 to improve light extraction efficiency. The depressions 22 are formed in such a manner that a tantalum oxide (Ta_2O_5) film 24 formed at an even thickness on the upper main surface of the n-AlGaN layer 14 is partially removed by etching. A Ti/Pt/Au electrode 26 which is L-shaped is formed in an area on the upper main surface of the n-AlGaN layer 14.

0019

An insulating film 28 made of silicon nitride is formed on the entire surface of each side surface of the multilayer epitaxial structure 6 and in an area of the upper main surface of the multilayer epitaxial structure 6 (so as to frame the upper main surface of the multilayer epitaxial structure 6).

An anode power supply terminal 30 and a cathode power supply terminal 32 which are made of Ti/Au are formed on a lower main surface of the Si substrate 4 which is opposite to a main surface on which the multilayer epitaxial structure 6 is formed.

The conductive film 18 has a portion which is not covered by the multilayer epitaxial structure 6 (hereinafter referred to as an extended portion 18A). The extended portion 18A is used to electrically connect the conductive film 18 to the anode power supply terminal 30 by a through hole 34 provided in the Si substrate 4.

0020

A wiring 36 is connected at its one end to a corner portion 26A of the L-shaped electrode 26, and extends, from the corner portion 26A, to a periphery of the upper main surface of the n-AlGaN layer 14 (the light extraction surface of the multilayer epitaxial structure 6) and then runs along a side surface of the multilayer epitaxial structure 6, to reach the Si substrate 4. The wiring 36 is made up

of a Ti/Pt/Au film, and electrically insulated from the multilayer epitaxial structure 6 by means of the insulating film 28. The wiring 36 is electrically connected at the other end to the cathode power supply terminal 32 by a through hole 38 provided in the Si substrate 4. Here, the through holes 34 and 38 are each formed by filling a through hole running in a thickness direction of the Si substrate 4 with Pt.

0021

The phosphor film 8 covers the side surfaces and the light extraction surface of the multilayer epitaxial structure 6 formed on the Si substrate 4. The light extraction surface is the upper main surface of the multilayer epitaxial structure 6 which is opposite to a main surface to which the Si substrate 4 is connected. The phosphor film 8 is made of a light-transmitting resin such as silicone in which particles of phosphors of four different colors and fine particles of metal oxide such as SiO_2 are dispersed. Such phosphors include a blue phosphor which contains at least one of $(Ba, Sr)MgAl_{10}O_{17}:Eu^{2+}$, $(Ba, Sr, Ca, Mg)_{10}(PO_4)_6Cl_2:Eu^{2+}$ and the like, a green phosphor which contains at least one of $BaMgAl_{10}O_{17}:Eu^{2+}Mn^{2+}$, $(Ba, Sr)_2SiO_4:Eu^{2+}$ and the like, a yellow phosphor which contains, for example, $(Sr, Ba)_2SiO_4:Eu^{2+}$, and a red phosphor which contains at least one of $La_2O_2S:Eu^{3+}$, $CaS:Eu^{2+}$, $Sr_2Si_5N_8:Eu^{2+}$ and the like. Instead of silicone, an epoxy resin or a polyimide resin may be used as the light-transmitting resin. The phosphor film 8 is formed on and around the multilayer epitaxial structure 6 at a substantially even thickness.

0022

An Al light reflective film 40 is formed between the phosphor film 8 and an area, on the Si substrate 4, in which the multilayer epitaxial structure 6 is not formed.

When power is supplied to the LED chip 2 described above through

the anode and cathode power supply terminals 30 and 32, the light emitting layer 12 of the multilayer epitaxial structure 6 emits near-ultraviolet light having a wavelength of 390 nm. The near-ultraviolet light from the light emitting layer 12 is, to a large extend, emitted from the n-AlGaN layer 14 and absorbed in the phosphor film 8. The phosphor film 8 converts the near-ultraviolet light into white light.

0023

As mentioned earlier, while the multilayer epitaxial structure 6 only has a thickness of less than 3 μm, the phosphor film 8 has a comparatively large thickness of 200 μm. In addition, the phosphor film 8 is also formed on the side surfaces of the multilayer epitaxial structure 6. Here, the phosphor film 8 is formed on and around the multilayer epitaxial structure 6 at a substantially even thickness. Accordingly, the LED chip 2 can produce white light with little unevenness of color, which is caused by variance in thickness of the phosphor film 8.

0024

According to present embodiment, the high-reflective electrode 16 is formed as a p-electrode in the LED chip 2. This significantly improves light extraction efficiency of the multilayer epitaxial structure 6. The light extraction efficiency of the multilayer epitaxial structure 6 can be also improved by the depressions 22 formed in the tantalum oxide film 24 on the upper main surface of the n-AlGaN layer 14, which is the light extraction surface. Furthermore, the light reflective film 40 improves the light extraction efficiency of the LED chip 2.

0025

Furthermore, a sapphire substrate or the like is not provided on the light extraction side of the multilayer epitaxial structure

6 in the LED chip 2. Accordingly, the LED chip 2 has much higher light extraction efficiency than an LED chip in which light emitted from a light emitting layer is emitted outside through a sapphire substrate or the like. According to the embodiment, the p-electrode (the high-reflective electrode 16) is formed on the substantially entire surface of a p-type layer (the p-AlGaN layer 10) which is difficult to be configured to have a low resistance. This enables an electric current to be evenly injected to the entire multilayer semiconductor layer 6, thereby making it possible that the entire light emitting layer 12 evenly emit light and that a lower operation voltage is achieved.

0026

To mount the LED chip 2, the power supply terminals 30 and 32 are directly connected to pads formed on a mounting substrate as described later. Here, having the phosphor film 8, the LED chip 2 can emit white light by itself. This makes it possible to test the LED chip 2 for its optical performance as described above before the LED chip 2 is mounted. As a result, it can be prevented that a finished product including the mounting board on which the LED chip 2 has been mounted is rejected due to the optical performance of the LED chip 2. In this way, the ratio of accepted finished products can be improved. In addition, the LED chip 2 relating to the embodiment can be made smaller, when compared with the above-mentioned conventional LED chip which requires an auxiliary mounting substrate in addition to a base substrate that directly supports a multilayer epitaxial structure.

0027

Furthermore, the anode and cathode power supply terminals 30 and 32 are positioned below the multilayer epitaxial structure 6 in the LED chip 2. Therefore, when the LED chip 2 is mounted, no components that block light, such as a bonding wire, exist on or above the light

extraction surface of the multilayer epitaxial structure 6. Therefore, light emitted from the LED chip 2 does not contain shadow.

The following part explains a manufacturing method for the LED chip 2 described above with reference to Figs. 2 to 7. In Figs. 2 to 7, a material to form each constituent of the LED chip 2 is identified by a five-digit number whose first digit is one. The last four digits of the five-digit number represents a reference numeral identifying the corresponding constituent of the LED chip 2.

0028

Firstly, as shown in Fig. 2, an n-AlGaN layer 1014, an InGaN/AlGaN MQW light emitting layer 1012, and a p-AlGaN layer 1010 are formed by epitaxial growth on the sapphire substrate 42, which is a single-crystal substrate, in the stated order using a MOCVD method (step A2). Here, the sapphire substrate 42 has a diameter of two inches and a thickness of 300 μm.

0029

After this, a mask is formed on a multilayer epitaxial structure 1006 composed of the layers 1014, 1012 and 1010, and an unmasked area of the multilayer epitaxial structure 1006 is removed by dry etching to such a depth that the sapphire substrate 42 is exposed. Thus, multilayer epitaxial structures 6, each of which constitutes the LED chip 2 (shown in Fig. 1B), are formed on the sapphire substrate 42 (step B2).

Subsequently, an Rh/Pt/Au film is formed by a technique such as an electron beam evaporation method, on the upper main surface of each multilayer epitaxial structure 6 (i.e. on the p-AlGaN layer 10). Thus, the high-reflective electrode 16 is formed (step C2).

0030

In parallel to the steps A2 to C2, steps D2 to E2 shown in Fig. 3 are conducted.

Holes 44 and 46 are created by dry etching in a high-resistive Si substrate 1004 in a thickness direction of the substrate 1004. The holes 44 and 46 are filled with Pt by electroless deposition, to form the through holes 34 and 38 (step D2).

0031

After this, a Ti/Pt/Au film is applied in a predetermined area on an upper main surface of the Si substrate 1004, to form the conductive film 18. In addition, an Au/Sn film is formed on a predetermined area on the conductive film 18, to form the connection layer 20 (step E2).

Subsequently, the sapphire substrate 42 is placed on the Si substrate 1004 so as that the high-reflective electrode 16 formed on the sapphire substrate 42 is in contact with the connection layer 20 formed on the Si substrate 1004. Then, while being pressed together, the sapphire substrate 42 and the Si substrate 1004 are heated until the connection layer 20 reaches 300°C (step F2). Thus, the high-reflective electrode 16 and the connection layer 20 are eutectic-bonded.

0032

After the high-reflective electrode 16 and the connection layer 20 are bonded together, a step of separating the sapphire substrate 42 from the multilayer epitaxial structure 6 is conducted (step G2). In detail, a YAG laser third harmonic beam LB having a wavelength of 355 nm is irradiated to the sapphire substrate 42 and the Si substrate 1004 from a side of the sapphire substrate 42 in such a manner that the beam scans the entire surface of the sapphire substrate 42. The irradiated laser beam is not absorbed by the sapphire substrate 42, but only by an interface between the sapphire substrate 42 and the n-AlGaN layer 14. Here, heat is generated locally and breaks AlGaN bond around the interface. As a consequence, the sapphire substrate 42 is separated from the multilayer epitaxial structure 6 in terms

of crystal structure (step G2). However, the sapphire substrate 42 is still adhered to the multilayer epitaxial structure 6 by means of a layer including a metal Ga (a pyrolytic layer). To separate the sapphire substrate 42 from the multilayer epitaxial structure 6 completely, the sapphire substrate 42 and the multilayer epitaxial structure 6 are immersed into hydrochloride or the like to dissolve the interface portion (step H2). It should be noted that the YAG laser third harmonic beam can be replaced with a KrF excimer laser having a wavelength of 248 nm or a mercury emission line having a wavelength of 365 nm.

0033

The multilayer epitaxial structure 6 is transferred from the sapphire substrate 42 to the Si substrate 1004 by separating the sapphire substrate 42 in the above-described manner. This eliminates internal stress within the multilayer epitaxial structure 6 generated by a difference in lattice constant between the n-AlGaN layer 14 and the sapphire substrate 42. As a result, distortion of the multilayer epitaxial structure 6 can be reduced. Furthermore, instead of the substrate 4 supporting the multilayer epitaxial structure 6 in the LED chip 2, a substrate selected from more extensive options including a substrate that has higher heat dissipation (higher heat conductivity) than a substrate used for epitaxial growth can be used as a base substrate.

0034

In the following step I2, a silicon nitride film is formed by high-frequency sputtering or the like for insulation and surface protection, to form the insulating film 28. Here, the silicon nitride film is formed on the upper main surface of the multilayer epitaxial structure 6 (the n-AlGaN layer 14) along its periphery, on the side surfaces of the multilayer epitaxial structure 6, and on the extended

portion 18A of the conductive film 18.

After this, a Ti/Pt/Au film is applied, to form the electrode 26 and the wiring 36 (step J2) as one unit.

0035

An Al film is applied, to form the light reflective film 40 (step K2).

After this, the tantrum oxide (Ta_2O_5) film 24 is deposited by sputtering or the like on a part of the main surface of the n-AlGaN layer 14 which is not covered by the electrode 26, the insulating film 28 and the wiring 36. Then, the tantrum oxide film 24 is partially removed by etching, to form the depressions 22 (step L2).

Subsequently, a first macromolecule film 48 is adhered to a front main surface, of the Si substrate 1004, on which the multilayer epitaxial structure 6 is formed, by means of a polyester adhesive layer (not illustrated) (step M2). When heated, the adhesive layer foams and loses adhesivity.

0036

After this, a back main surface of the Si substrate 1004 is polished so that the thickness of the Si substrate 1004 becomes 100 μm (step N2). Thus, the through holes 34 and 38 are exposed on the back main surface of the Si substrate 1004.

Following this, a Ti/Au film is applied in a predetermined area on the back main surface of the Si substrate 1004, to form the anode and cathode power supply terminals 30 and 32 (step O2).

0037

The first macromolecule film 48 that has been adhered to the front main surface of the Si substrate 1004 is then removed. A second macromolecule film 50 is adhered to the back main surface of the Si substrate 1004 as a dicing sheet (step P2).

Lastly, after the phosphor film 8 is formed by screen printing

(step Q2), the Si substrate 1004 is diced by a dicing blade DB into individual LED chips 2 (step R2). Thus, the LED chip 2 is manufactured.

<Second Embodiment>

According to the first embodiment, the anode and cathode power supply terminals 30 and 32 are formed on the back main surface of the Si substrate 4, which is a base substrate, in the LED chip 2. In a white LED chip 102 relating to the second embodiment, however, one power supply terminal (an anode power supply terminal in the second example) is formed on a back main surface of a base substrate, and the other power supply terminal (a cathode power supply terminal in the second example) is formed on a front main surface of the base substrate.

0038

The LED chip 102 is the same as the LED chip 2, in terms of a composition and a thickness of each of layers constituting a multilayer epitaxial structure, and a composition of a phosphor film. However, the LED chip 102 is different from the LED chip 2 in terms of a construction of electrodes formed on both main surfaces of the multilayer epitaxial structure. In addition, the multilayer epitaxial structure of the LED chip 102 is formed on the base substrate in the same manner as the multilayer epitaxial structure 6. In detail, the multilayer epitaxial structure is first formed on a single-crystal substrate which is different from the base substrate, and then transferred to the base substrate.

Fig. 8A is a plan view illustrating the LED chip 102 relating to the second embodiment, and Fig. 21B illustrates a cross-section of the LED chip 102 along a line GG shown in Fig. 8A. Fig. 8A shows the LED chip 102 after removing a phosphor film 108 (shown in Fig. 8B).

0039

As shown in Figs. 8A and 8B, the LED chip 102 is formed in such a manner that a multilayer epitaxial structure 106 and the phosphor film 108 are formed on an n-type SiC substrate 104, which is a base substrate (hereinafter referred to as "an SiC substrate 104"). A main surface of the SiC substrate 104 is slightly larger than a main surface of the multilayer epitaxial structure 106. The multilayer epitaxial structure 106 is provided on one of the main surfaces of the SiC substrate 104 with a space being retained along a periphery of the substrate 104.

0040

The multilayer epitaxial structure 106 is made up of a p-AlGaN layer 110, an InGaN/AlGaN MQW light emitting layer 112, and an n-AlGaN layer 114. The layer 110 is the closest to the SiC Substrate 104, and then the layers 112 and 114 are formed in the stated order. Thus, the multilayer epitaxial structure 106 has a diode structure.

A multilayer dielectric film 116 made of SiO_2/Ta_2O_5 and a high-reflective electrode 118 made of Rh/Pt/Au are formed on a back main surface of the p-AlGaN layer 110. The multilayer dielectric film 116 is formed by partially removing a sheet-like multilayer dielectric film by etching with a predetermined pattern. The p-AlGaN layer 110 is electrically connected to the high-reflective electrode 118 in areas which are not covered by the multilayer dielectric film 116. A conductive film 120 is formed on an upper main surface of the SiC substrate 104 so as to correspond to the high-reflective electrode 118. The conductive film 120 is made of Ti/Pt/Au, and is connected to the high-reflective electrode 118 by a connection layer 122 which is made of a conductive material such as Au/Sn. A Ti/Au anode power supply terminal 124 is formed on the entire back main surface of the SiC substrate 104. Thus, the high-reflective electrode 118 is

electrically connected to the anode power supply terminal 124 by means of the connection layer 122, the conductive film 120 and the SiC substrate 104.

0041

An ITO transparent electrode 126 and an SiO_2/Ta_2O_5 multilayer dielectric film 128 are formed in this order on an upper main surface of the n-AlGaN layer 114.

An SiO_2 insulating film 130 is formed on an area, on the upper main surface of the SiC substrate 104, in which the multilayer epitaxial structure 106 is not formed. An insulating film 132 made of silicon nitride is formed on the side surfaces of the multilayer epitaxial structure 106 and on a part of an upper main surface of the multilayer epitaxial structure 106 (so as to frame the upper main surface).

0042

As shown in Fig. 8A, a rectangular cathode power supply terminal 134 formed by a Ti/Pt/Al film is provided on the insulating film 130.

A side of the ITO transparent electrode 126 and a side of the cathode power supply terminal 134 are connected to each other by means of a wiring 136 that is formed along the side surface of the multilayer epitaxial structure 106. The wiring 136 is formed by a Ti/Pt/Al film, and electrically insulated from the multilayer epitaxial structure 106 by the insulating film 132.

0043

A light reflective film 138 of a Ti/Pt/Al film is formed so as to surround the multilayer epitaxial structure 106 on the insulating film 130. The light reflective film 138 is substantially U-shaped.

The phosphor film 108 covers the side surfaces of the multilayer epitaxial structure 106 and a main surface (a light extraction surface) of the multilayer epitaxial structure 106 which is opposite to a main surface to which the SiC substrate 104 is connected. As shown in Fig.

21B, a large portion of the cathode power supply terminal 134 is not covered by the phosphor film 108.

0044

When power is supplied to the LED chip 102 described above through the anode and cathode power supply terminals 124 and 134, the light emitting layer 112 in the multilayer epitaxial structure 106 emits near-ultraviolet light having a wavelength of 390 nm.

In the LED chip 102 relating to the second embodiment, the multilayer epitaxial structure 106 is positioned between mirror structures, i.e. the multilayer dielectric films 116 and 128. The mirror structure closer to the p-AlGaN layer 110 has a reflectance of 99% or over, and the mirror structure closer to the n-AlGaN layer 114 has a reflectance of 90% or over. Thus, a resonant LED structure is formed. The near-ultraviolet light having a wavelength of 390 nm emitted from the light emitting layer 112 is emitted through the multilayer dielectric film 128, which is the mirror structure closer to the n-AlGaN layer 114 and has a lower reflectance, and absorbed by the phosphor film 108. The phosphor film 108 converts the near-ultraviolet light into white light.

0045

Having a resonant LED structure, the LED chip 102 relating to the second embodiment has a better light extraction efficiency in a direction perpendicular to the light emitting layer 112. Generally speaking, if the thickness of the p-AlGaN layer 110 and that of the n-AlGaN layer 114 are reduced, an electric current is likely to expand in a horizontal direction unevenly. This may cause light to be emitted unevenly from the light emitting layer 112. The uneven light emission becomes more notable as a light emission area becomes large. According to the second embodiment, power is supplied to the p-AlGaN layer 110 through the high-reflective electrode 118. Here, the electrode 118

is formed on the substantially entire surface of the p-AlGaN layer 110 since the multilayer dielectric film 116 is formed by partially etching a sheet-like multilayer dielectric film. Furthermore, power is supplied to the n-AlGaN layer 114 through the ITO transparent electrode 126. Here, the electrode 126 is formed on the entire main surface of the n-AlGaN layer 114. Thus, an electric current can be evenly injected to the entire light emitting layer 112. This enables the entire light emitting layer 112 evenly emit light, with it being possible to achieve a lower operation voltage. In addition, since the LED chip 102 does not include an insulating substrate such as a sapphire substrate, an ability to withstand static electricity is improved.

0046

To mount the LED chip 102, the anode power supply terminal 124 is directly connected to a pad formed on a mounting substrate, and the cathode power supply terminal 134 is connected to another pad by a bonding wire. The second embodiment can achieve the same effects as the first embodiment. In detail, having the phosphor film 108, the LED chip 102 can emit white light by itself. This makes it possible to test the LED chip 102 for its optical performance as described above before the LED chip 102 is mounted. As a result, it can be prevented that a finished product including the mounting board on which the LED chip 102 is mounted is rejected due to the optical performance of the LED chip 102. In this way, the ratio of accepted finished products can be improved. In addition, the LED chip 102 relating to the second embodiment can be made smaller, when compared with the above-mentioned conventional LED chip which requires an auxiliary mounting substrate in addition to a base substrate that directly supports a multilayer epitaxial structure.

0047

In the LED chip 102, the anode power supply terminal 124 is formed on the back main surface of the SiC substrate 104, and the cathode power supply terminal 134 is formed on the upper main surface of the SiC substrate 104. Which is to say, the both anode and cathode power supply terminals 124 and 134 are positioned closer to the SiC substrate 104 than the light extraction surface of the multilayer epitaxial structure 106. The anode power supply terminal 124 is electrically connected to a p-electrode (the high-reflective electrode 118) by the SiC substrate 104. The cathode power supply terminal 134 is connected to an n-electrode (the ITO transparent electrode 126) by the wiring 136 that extends from the ITO transparent electrode 126 towards the side surface of the n-AlGaN layer 114. When the LED chip 102 is mounted, no components that block light, such as a bonding wire, exist on or above the light extraction surface of the multilayer epitaxial structure 106. Therefore, light emitted from the LED chip 102 does not contain shadow.

0048

The following part explains a manufacturing method for the LED chip 102 described above, with reference to Figs. 9 to 14. In Figs. 9 to 14, a material to form each constituent of the LED chip 102 is identified by a four-digit number whose first digit is "2". The last three digits of the four-digit number represents a reference numeral identifying the corresponding constituent of the LED chip 102.

Firstly, as shown in Fig. 9, an n-AlGaN layer 2114, an InGaN/AlGaN MQW light emitting layer 2112, and a p-AlGaN layer 2110 are formed by epitaxial growth on a sapphire substrate 140, which is a single-crystal substrate, in the stated order using a MOCVD method (step A3). Here, the sapphire substrate 140 has a diameter of two inches and a thickness of 300 μm.

0049

After this, a mask is formed on a multilayer epitaxial structure 2106 composed of the layers 2114, 2112 and 2110, and an unmasked are of the multilayer epitaxial structure 2106 is removed by dry etching to such a depth that the sapphire substrate 140 is exposed. Thus, multilayer epitaxial structures 106, each of which constitutes the LED chip 102 (shown in Fig. 8B) are formed on the sapphire substrate 140 (step B3).

Subsequently, an SiO_2/Ta_2O_5 multilayer dielectric film is formed on an upper main surface of each multilayer epitaxial structure 106 (the p-AlGaN layer 110) by RF sputtering or the like. The SiO_2/Ta_2O_5 multilayer dielectric film is partially removed by etching to such a depth that the p-AlGaN layer 110 is exposed, to form the multilayer dielectric film 116 (step C3). On the multilayer dielectric film 116, an Rh/Pt/Au film is applied by a technique such as an electron beam evaporation method. Thus, the high-reflective electrode 118 is formed (step D3).

0050

In parallel to the steps A3 to D3, a step E3 shown in Fig. 10 is conducted.

After an SiO_2 film is formed on one of main surfaces of an n-type SiC substrate 2104 so as to cover the entire surface, an area of the SiO_2 film in which the conductive film 120 is to be formed is removed. Thus, the insulating film 130 is formed. After this, a Ti/Pt/Au film is applied in the SiO_2-film removed area, to form the conductive film 120. On the conductive film 120, an Au/Sn film 2122 is formed (step E3).

0051

After this, the sapphire substrate 140 is placed on the SiC substrate 2104 so as that the high-reflective electrode 118 formed on the sapphire substrate 140 is in contact with the Au/Sn film 2122

formed on the SiC substrate 2104. Then, while being pressed together, the sapphire substrate 140 and the SiC substrate 2104 are heated until the Au/Sn film 2122 reaches 300°C (step F3). Thus, the high-reflective electrode 118 and the Au/Sn film 2122 are eutectic-bonded. Consequently, since the Au/Sn film 2122 is processed to be the connection layer 122, the high-reflective electrode 118 and the conductive film 120 are physically and electrically connected together.

0052

After the high-reflective electrode 118 and the connection layer 122 are bonded together, steps G3 and H3 (shown in Fig. 11) are conducted to separate the sapphire substrate 140 from the multilayer epitaxial structure 106. The steps G3 and H3 are the same as the steps G2 and H2 (shown in Fig. 4) described in the first embodiment, and therefore not repeatedly explained here.

In the steps G3 and H3, the sapphire substrate 140 is separated, and the multilayer epitaxial structure 106 and the like are transferred from the sapphire substrate 140 to the SiC substrate 2104. In the next step I3, an upper main surface of the n-AlGaN layer 114 which is opposite to a lower main surface to which the light emitting layer 112 is connected is flattened using a mechanical or a chemical process. After this, an ITO film is applied on the upper main surface of the n-AlGaN layer 114 by sputtering or the like, to form the ITO transparent electrode 126.

0053

On the ITO transparent electrode 126, the multilayer dielectric film 128 is formed by sputtering or the like (step J3).

The insulating film 132 is formed by applying a silicon nitride film by sputtering or the like (step K3).

After this, a Ti/Pt/Al film is deposited in predetermined areas on the resulting surface after the step K3, to form the cathode power

supply terminal 134, the wiring 136, and the light reflective film 138 simultaneously (step L3).

0054

Subsequently, a first macromolecule film 142 is adhered to a front main surface, of the SiC substrate 2104, on which the multilayer epitaxial structure 106 is formed, similarly to the first embodiment (step M3).

After this, a back main surface of the SiC substrate 2104 is polished so that the thickness of the SiC substrate 2104 becomes 100 μm. A Ti/Au film 2124 is then applied on the back main surface of the SiC substrate 2104, to form the anode power supply terminal 124 (shown in Fig. 8B) (step N3).

0055

The first macromolecule film 142 that has been adhered to the front main surface of the SiC substrate 2104 is then removed. A second macromolecule film 144 is adhered to the back main surface of the SiC substrate 2104 as a dicing sheet (step O3).

Lastly, after the phosphor film 108 is formed by screen printing (step P3), the SiC substrate 2104 is diced by a dicing blade DB into individual LED chips 102 (step Q3). Thus, the LED chip 102 is manufactured.

<Third Embodiment>

Fig. 15A is a plan view illustrating a white LED array chip 202 which is one type of a semiconductor light emitting device (hereinafter referred to as "an LED array chip 202"), Fig. 15B illustrates a cross-section of the LED array chip 202 along a line HH shown in Fig. 15A, and Fig. 15C illustrates how LEDs are connected in the LED array chip 202. Fig. 15A shows the LED array chip 202 after removing a phosphor film 208 (shown in Fig. 15B and mentioned later). A cross-section

along each of a line EE and a line FF shown in Fig. 15A is the same as the cross-section shown in Fig. 15B.

0056

The LED array chip 202 is formed in such a manner that nine LED D01 to D09 are arranged in a matrix of 3×3 as shown in Fig. 15A. The LED array chip 202 is a square approximately 1.2 mm on a side. The LEDs D1 to D9 each have the same construction as the LED chip 2 relating to the first embodiment, except for a pattern of depressions formed in order to improve light extraction efficiency and a construction of an n-electrode. The LEDs D1 to D9 are connected in series-parallel in the LED array chip 202 as shown in Fig. 15C. In detail, the LEDs D1 to D9 are divided into groups each of which has three LEDs connected in series in a row direction, and the groups are connected in parallel. It is mentioned later how adjacent LEDs are connected to each other in the LED array chip 202.

0057

As shown in Fig. 15B, the LED array chip 202 includes an AlN substrate 204 as a base substrate to support a multilayer epitaxial structure 206.

The multilayer epitaxial structure 206 constituting each of the LEDs D1 to D9 is made up of a p-AlGaN layer 210, an InGaN/AlGaN MQW light emitting layer 212, and an n-AlGaN layer 214 as in the LED chip 2 relating to the first embodiment shown in Fig. 1B. The layer 210 is the closest to the AlN substrate 204, and then the layers 212 and 214 are formed in the stated order. On a lower main surface of the p-AlGaN layer 210, an Rh/Pt/Au p-electrode 216, which is a high-reflective electrode, is formed. On an upper main surface of the AlN substrate 204, a Ti/Pt/Au conductive film 218 is formed. The conductive film 218 and the p-electrode 216 are physically and electrically connected to each other by means of an Au/Sn connection

layer 220. An upper main surface of the n-AlGaN layer 214 (i.e. a light extraction surface of the multilayer epitaxial structure 206) is made uneven, to have depressions 222. This is aimed at improving light extraction efficiency.

0058

A Ti/Pt/Al n-electrode 226 is formed along one side of the upper main surface of the n-AlGaN layer 214 of each multilayer epitaxial structure 206. An insulating film 228 made of silicon nitride is formed so as to cover side surfaces and a part of an upper main surface of the multilayer epitaxial structure 206.

The following part describes how the LEDs D4 to D6 are connected in series.

The LEDs D4, D5 and D6 are connected in series in this order in the following manner. A conductive film 218 of the LED D4 is connected to an n-electrode 226 of the LED D05 by a bridging wire 234A. A conductive film 218 of the LED D5 is connected to an n-electrode 226 of the LED D6 by a bridging wire 234B. In the same manner, the LEDs D1, D2 and D3 are connected in series in this order, and the LEDs D7, D8 and D9 are connected in series in this order.

0059

A Ti/Pt/Al cathode power supply terminal 230 is formed in a left-half area of the upper main surface of the AlN substrate 204, and a Ti/Pt/Al anode power supply terminal 232 is formed in a right-half area.

An n-electrode 226 of the LED D4 is electrically connected to the cathode power supply terminal 230 by a wiring 236A. In the same manner, n-electrodes 226 of the LEDs D1 and D7 are connected to the cathode power supply terminal 230. Thus, the n-electrodes 226 of the LEDs D1, D4 and D7 are electrically connected in parallel.

0060

A conductive film 218 of the LED D6 extends so as to overlap the anode power supply terminal 232 and to be connected to the anode power supply terminal 232 at the overlap. In the same manner, conductive films 218 of the LEDs D3 and D9 are connected to the anode power supply terminal 232. Thus, the p-electrodes 216 of the LEDs D3, D6 and D9 are electrically connected in parallel.

As seen from the above description, the cathode and anode power supply terminals 230 and 232 also function as a wiring to connect, in parallel, the groups of the LEDs that are connected in series. The cathode and anode power supply terminals 230 and 232 cover a major part of an area, on the upper main surface of the AlN substrate 204, in which the multilayer epitaxial structures 206 are not formed, and also function as a light-reflective film.

0061

As described above, the nine LEDs D1 to D9 are connected in series-parallel and arranged in a matrix on the AlN substrate 204 so that a space is left along edges of the AlN substrate 204. The phosphor film 208 covers side surfaces and the light extraction surface of each of the LEDs D1 to D9 (the multilayer epitaxial structures 206) formed on the AlN substrate 204. Here, the phosphor film 208 may have the same composition as the phosphor film 8 relating to the first embodiment.

0062

A Ti/Au film 238 is formed on a back main surface of the AlN substrate 204.

When power is supplied to the LED array chip 202 described above through the cathode and anode power supply terminals 230 and 232, the light emitting layer 212 of each of the LEDs D1 to D9 emits near-ultraviolet light having a wavelength of 390 nm. The near-ultraviolet light emitted from the light emitting layer 212 is,

to a large extent, emitted from the n-AlGaN layer 214 and absorbed by the phosphor film 208. The phosphor film 208 converts the near-ultraviolet light into white light.

0063

In the LED array chip 202, the p-electrode 216 is formed as a high-reflective electrode, and the depressions 222 are formed on the upper main surface of the n-AlGaN layer 214 (the light extraction surface). These constructions contribute to significantly improve the light extraction efficiency of the multilayer epitaxial structure 206. The cathode and anode power supply terminals 230 and 232 function as a light-reflective film. This construction contributes to improve light extraction efficiency of the LED array chip 202.

0064

To mount the LED array chip 202, the Ti/Au film 238 is directly connected to a pad formed on a mounting substrate. The cathode power supply terminal 230 and the anode power supply terminals 232 are each connected to a power-supply pad formed on the mounting substrate by wire bonding.

Here, since the LED array chip 202 includes the phosphor film 208, the LED array chip 202 can emit white light by itself. This and other features of the LED array chip 202 produce the same effects as the first and second embodiments.

0065

The following part describes a manufacturing method for the LED array chip 202 described above, with reference to Figs. 16 to 19. In Figs. 16 to 19, a material to form each constituent of the LED array chip 202 is identified by a four-digit number whose first digit is "3". The last three digits of the four-digit number represents a reference numeral identifying the corresponding constituent of the LED chip 202.

Firstly, as shown in Fig. 16, an n-AlGaN layer 3214, an InGaN/AlGaN MQW light emitting layer 3212, and a p-AlGaN layer 3210 are formed by epitaxial growth on a sapphire substrate 240, which is a single-crystal substrate, in the stated order using a MOCVD method (step A4). Here, the sapphire substrate 240 has a diameter of two inches and a thickness of 300 μm.

0066

After this, a mask is formed on a multilayer epitaxial structure 3206 composed of the layers 3214, 3212 and 3210, and an unmasked area of the multilayer epitaxial structure 3206 is removed by dry etching to such a depth that the sapphire substrate 240 is exposed. Thus, multilayer epitaxial structures 206, which constitute the LED array chip 202 (shown in Fig. 15B), are formed on the sapphire substrate 240 (step B4).

Subsequently, an Rh/Pt/Au film is formed by a technique such as an electron beam evaporation method, on the upper main surface of each multilayer epitaxial structure 206 (i.e. the p-AlGaN layer 210). Thus, the p-electrode 216 is formed (step C4).

0067

In parallel to the steps A4 to C4 in Fig. 16, a step D4 shown in Fig. 17 is conducted.

In the step D4 shown in Fig. 17, a Ti/Pt/Au film is applied in a predetermined area on an upper main surface of an AlN substrate 3204, to form the conductive film 218. An Au/Sn film 3220 is applied on part of the conductive film 218, to form the connection layer 220. A Ti/Au film 2238 is plated on the entire back main surface of the AlN substrate 3204.

0068

After this, the sapphire substrate 240 is placed on the AlN substrate 3204 so that the p-electrode 216 formed on the sapphire

substrate 240 is in contact with the Au/Sn film 3220 formed on the AlN substrate 3204. Then, while being pressed together, the sapphire substrate 240 and the AlN substrate 3204 are heated until the Au/Sn film 3220 reaches approximately 300°C (step E4). Thus, the p-electrode 3216 and the Au/Sn film 3220 are eutectic-bonded together. Since the Au/Sn film 3220 is processed to be the connection layer 220, the p-electrode 216 and the conductive film 218 are physically and electrically connected together.

0069

After the p-electrode 216 and the conductive film 218 are bonded together by the connection layer 220, steps F4 and G4 (shown in Figs. 17 and 18) are conducted to separate the sapphire substrate 240 from the multilayer epitaxial structure 206. The steps F4 and G4 are the same as the steps G2 and H2 (shown in Fig. 4) described in the first embodiment, and therefore not repeatedly explained here.

After the sapphire substrate 240 is separated and the multilayer epitaxial structure 206 and the like are transferred from the sapphire substrate 240 to the AlN substrate 3204 as describe above, a step H4 (shown in Fig. 18) is conducted. In the step H4, a silicon nitride film is formed by high-frequency sputtering or the like for insulation and surface protection, to form the insulating film 228. Here, the silicon nitride film is formed along a periphery of the upper main surface of the multilayer epitaxial structure 206 (the n-AlGaN layer 214), and on the side surfaces of the multilayer epitaxial structure 206.

0070

After this, anisotropic etching is conducted, using KOH solution or the like, to an area of the upper main surface of the n-AlGaN layer 214 in which the insulating film 228 is not formed. Thus, the depressions 222 are formed (step I4).

Subsequently, a Ti/Pt/Al film is applied in predetermined areas on the resulting surface after the step I4, to form the n-electrode 226, the bridging wire 234, the wiring 236, and the cathode and anode power supply terminals 230 and 232 simultaneously (step J4).

0071

After the phosphor film 208 is formed by screen printing (step K4), a macromolecule film 242 is adhered to the back main surface of the AlN substrate 3204 as a dicing sheet. Lastly, the AlN substrate 3204 is diced by a dicing blade DB into individual LED array chips 202 (step L4). Thus, the LED array chip 202 is manufactured.

According to the third embodiment, the LED array chip 202 includes the nine LEDs D1 to D9 (light emitting elements), and is a square approximately 1.2 mm on a side. However, the third embodiment is not limited to such. The LED array chip 202 may include any number of LEDs (light emitting elements).

<Fourth Embodiment>

Fig. 20 is an external perspective view illustrating a white LED module 300 including LED chips 2 relating to the first embodiment (shown in Fig. 1B). This LED module 300 is attached to a lighting unit 332 (mentioned later and shown in Figs. 23A and 23B).

0072

The LED module 300 includes a ceramics substrate 302 that is in a shape of a circle having a diameter of 5 cm and is made of AlN and 217 pieces of resin lenses 304. A guiding depression 306 used to attach the LED module 300 to the lighting unit 332 and terminals 308 and 310 to receive a power supply from the lighting unit 332 are provided in the ceramics substrate 302.

Fig. 21A is a plan view illustrating the LED module 300, Fig. 21B illustrates a cross-section of the LED module 300 along a line

GG shown in Fig. 21A, and Fig. 21C is an enlargement view illustrating a chip mounted area shown in Fig. 21B.

0073

As shown in Fig. 21C, a gold plating 312 is applied to a back main surface of the ceramics substrate 302 for improving heat dissipation.

The LED chip 2 is mounted at a location, on an upper surface of the ceramics substrate 302, corresponding to a center of each of the lenses 304 having a shape of a circle as shown in Fig. 21A. In total, 217 pieces of LED chips 2 are mounted on the ceramics substrate 302.

The ceramics substrate 302 is constituted by two ceramics substrates 314 and 316 each of which is 0.5 mm in thickness and mainly made of AlN. Other than AlN, the ceramics substrate 314 and 316 can be made of Al_2O_3, BN, MgO, ZnO, SiC or diamond.

0074

The LED chips 2 are mounted on the lower ceramics substrate 316. Taper through holes 318 are provided in the upper ceramics substrate 314, so as to create spaces for mounting the LED chips 2.

A cathode pad 320 and an anode pad 322 (shown in Fig. 22B) are provided at the location, on an upper surface of the ceramics substrate 316, where each LED chip 2 is to be mounted. Each of the cathode pad 320 and the anode pad 322 is made up of Au plating applied on copper (Cu). Here, the cathode power supply terminal 32 and the anode power supply terminal 30 of the LED chip 2 (shown in Fig. 1B) are respectively connected to the cathode pad 320 and the anode pad 322 on which PbSn solder has been formed.

0075

A step of forming the PbSn solder on the cathode pad 320 and the anode pad 322 can be omitted, if AuSn solder is plated beforehand

on the cathode power supply terminal 32 and the anode power supply terminal 30. After all of the LED chips 2 are mounted on pairs of the cathode pad 320 and the anode pad 322, the ceramics substrate 302 is heated through a reflow furnace to a temperature equal to a melting point of the solder. Thus, the 217 pieces of LED chips 2 can be simultaneously connected to the ceramics substrate 302. This reflow soldering process can be conducted if a shape of each of the cathode pad 320 and the anode pad 322, an amount of the applied solder, and a shape of the anode power supply terminal 30 and the cathode power supply terminal 32 are optimized. Here, a silver paste or a bump may be used instead of the solder.

0076

Before being mounted, the LED chips 2 have been tested for their optical performance, such as unevenness of color and a color temperature, and have passed the test. According to the fourth embodiment, the LED chip 2 includes the phosphor film 8, and can emit white light by itself. As described above, this makes it possible to test the LED chip 2 for its optical performance before mounting. Consequently, it can be prevented that the LED module 300 including the LED chips 2 is rejected due to poor optical performance of the LED chips 2. Consequently, the ratio of accepted finished products (LED modules 300) is improved.

0077

An aluminum reflection film 324 is formed on a wall of each through hole 318 provided in the upper ceramics substrate 314 and on an upper surface of the ceramics substrate 314 as shown in Fig. 21C.

After mounted on the ceramics substrate 316, the LED chips 2 are covered by a first resin (e.g. a silicone resin 326). Subsequently, the lenses 304 are formed by injection molding with use of a second resin (e.g. an epoxy resin 328).

0078

The 217 pieces of LED chips 2 are connected in series-parallel by a wiring pattern 330 (shown in Fig. 22A) formed on the upper main surface of the ceramics substrate 316.

Fig. 22A is a plan view illustrating the LED module 300 after removing the lenses 304 and the upper ceramics substrate 314. As describe above, the anode pad 322 and the cathode pad 320 (shown in Fig. 22B) are provided at the location, on the upper main surface of the ceramics substrate 316, where each LED chip 2 is to be mounted.

0079

The anode pads 322 and the cathode pads 320 are connected by the wiring pattern 330 in such a manner that 31 pieces of LED chips 2 are connected in series and seven groups of the 31 pieces of LED chips 2 are connected in parallel. The wiring pattern 330 is connected at one end to the positive terminal 308 (shown in Fig. 21A) by a through hole (not illustrated), and connected at the other end to the negative terminal 210 (shown in Fig. 21A) by another through hole (not illustrated).

0080

The LED module 300 described above is attached to the lighting unit 332. The LED module 300 and the lighting unit 332 constitute a lighting apparatus 334.

Fig. 23A is a schematic perspective view illustrating the lighting apparatus 334, and Fig. 23B is a bottom plan view illustrating the lighting apparatus 334.

0081

The lighting unit 332 is, for example, fixed on a ceiling of a room. The lighting unit 332 includes a power supply circuit (not shown in Figs. 23A and 23B) that converts alternating-current power (e.g. 100 V, 50/60Hz) supplied from a commercial power source into

direct-current power required for driving the LED module 300.

The following part describes a construction to attach the LED module 300 to the lighting unit 332, with reference to Fig. 24.

0082

The lighting unit 332 has a circular depression 336 in which the LED module 300 is to be fitted. A bottom surface of the circular depression 336 is flat. An internal thread (not illustrated) is created, in the vicinity of an open end of the circular depression 336, on an inside wall of the circular depression 336. Flexible power supply terminals 338 and 340 and a guiding protrusion 342 protrude from the inside wall of the circular depression 336, between the internal thread and the bottom surface of the circular depression 336. The power supply terminals 338 and 340 are respectively positive and negative.

0083

An O-ring 344 made of silicon rubber and a ring screw 346 are used to attach the LED module 300 to the lighting unit 332. The ring screw 346 has a shape of a ring that has a substantially rectangular cross-section. An external thread (not illustrated) is created on an outer surface of the ring screw 346, and a depression 346A is provided.

0084

The following part describes a procedure of attaching the LED module 300 to the lighting unit 332.

To start with, the LED module 300 is fitted in the circular depression 336 in the following manner. The ceramics substrate 302 of the LED module 300 is positioned between the bottom surface of the circular depression 336 and the power supply terminals 338 and 340. The guiding protrusion 342 is fitted in the guiding depression 306, so as to align the positive terminal 308 and the negative terminal 310 with the power supply terminal 338 and the power supply terminal 340 respectively.

0085

After the LED module 300 is fitted in the circular depression 336, the ring screw 346 to which the O-ring 344 has been attached is screwed into the circular depression 336 and fixed. Thus, the positive and negative terminals 308 and 310 are respectively connected to the power supply terminals 338 and 340, so that the terminals 308 and 310 are electrically connected to the terminals 338 and 340 reliably. In addition, the substantially entire lower surface of the ceramics substrate 302 is connected to the flat bottom surface of the circular depression 336. This enables heat generated in the LED module 300 to be effectively conducted to the lighting unit 332, thereby improving a cooling effect of the LED module 300. Here, silicone grease may be applied to the lower surface of the ceramics substrate 302 and the bottom surface of the circular depression 336 to further improve the heat conduction efficiency from the LED module 300 to the lighting unit 332.

0086

When power is supplied to this lighting apparatus 334 from a commercial power source, each LED chip 2 emits white light in the manner described above. The white light is emitted through the lenses 304.

When an electric current of 1 A is applied to the LED module 300, a total luminous flux of 4,000 lm, an on-axis luminous intensity of 10,000 cd, and an emission spectrum shown in Fig. 25 are observed.

0087

In the above description of the second embodiment, the semiconductor light emitting devices relating to the first to third embodiment are, as an example, used for lighting, such as a lighting module and a lighting apparatus. However, the semiconductor light emitting devices relating to the second embodiment may be also used

for display, to be specific, as a light source in a display element. Such a display element includes a surface mounting device (SMD) LED which is formed in such a manner that a semiconductor light emitting device (e.g. an LED chip) is mounted on a ceramics substrate and sealed by a transparent epoxy resin.

0088

For example, a single SMD LED may be used by itself. In this case, an SMD LED is mounted on a remote controller for a home electric appliance including a television, a video cassette recorder and an air conditioner, or used as a main switch lamp of such a home electric appliance. Alternatively, a plurality of SMD LEDs may be combined to be used as dots provided in a dot matrix display device for displaying a letter, a number, a symbol and the like.

0089

Up to now, preferred embodiments of the present invention have been described. However, not limited to the above-described embodiments, the present invention may take, for example, the following embodiments.

(1) According to the first to third modification examples of the second embodiment, a multilayer epitaxial structure is formed by epitaxial growth on a sapphire substrate which is a single-crystal substrate. In addition, the multilayer epitaxial structure is divided into individual LED (array) chips on the sapphire substrate (see step B2 in Fig. 2, step B3 in Fig. 9, and step B4 in Fig. 16). However, the second embodiment is not limited to such. Alternatively, the multilayer epitaxial structure as a whole may be first transferred to a base substrate (the high-resistive Si substrate 12004 in Fig. 16, the n-type SiC substrate 2104 in Fig. 10 and the AlN substrate 3204 in Fig. 17) which constitutes the LED (array) chip. The multilayer epitaxial structure is then divided into the individual LED (array)

chips on the base substrate.

[INDUSTRIAL APPLICABILITY]

0090

As describe above, a semiconductor light emitting device relating to the present invention is applicable to a lighting apparatus. This is because a light emitting device used for a lighting apparatus needs to be tested for its optical performance, for example, unevenness of color, before being mounted on the lighting apparatus.

[BRIEF DESCRIPTION OF THE DRAWINGS]

0091

Figs. 1A through 1C show an LED chip relating to the first embodiment. Fig. 1A is a plan view illustrating the LED chip after removing a phosphor film. Fig. 1B is a cross-section of the LED chip taken along a line AA shown in Fig. 1A. Fig. 1C is a bottom plan view of the LED chip.

Fig. 2 illustrates part of a manufacturing process of the LED chip relating to the first embodiment.

Fig. 3 illustrates part of the manufacturing process of the LED chip relating to the first embodiment.

Fig. 4 illustrates part of the manufacturing process of the LED chip relating to the first embodiment.

Fig. 5 illustrates part of the manufacturing process of the LED chip relating to the first embodiment.

Fig. 6 illustrates part of the manufacturing process of the LED chip relating to the first embodiment.

Fig. 7 illustrates part of the manufacturing process of the LED chip relating to the first embodiment.

Figs. 8A through 8B show an LED chip relating to the second

embodiment. Fig. 8A is a plan view illustrating the LED chip after removing a phosphor film. Fig. 8B is a cross-section of the LED chip along a line BB shown in Fig. 8A.

Fig. 9 illustrates part of a manufacturing process of the LED chip relating to the second embodiment.

Fig. 10 illustrates part of a manufacturing process of the LED chip relating to the second embodiment.

Fig. 11 illustrates part of a manufacturing process of the LED chip relating to the second embodiment.

Fig. 12 illustrates part of a manufacturing process of the LED chip relating to the second embodiment.

Fig. 13 illustrates part of a manufacturing process of the LED chip relating to the second embodiment.

Fig. 14 illustrates part of a manufacturing process of the LED chip relating to the second embodiment.

Figs. 15A through 15C show an LED chip relating to the third embodiment. Fig. 15A is a plan view illustrating the LED array chip after removing a phosphor film. Fig. 15B is a cross-section of the LED array chip along a line CC shown in Fig. 15A. Fig. 15C illustrates how LEDs are connected in the LED array chip.

Fig. 16 illustrates part of a manufacturing process of the LED chip relating to the third embodiment.

Fig. 17 illustrates part of a manufacturing process of the LED chip relating to the third embodiment.

Fig. 18 illustrates part of a manufacturing process of the LED chip relating to the third embodiment.

Fig. 19 illustrates part of a manufacturing process of the LED chip relating to the third embodiment.

Fig. 20 is a perspective view illustrating a white LED module relating to the fourth embodiment.

Fig. 21A is a plan view illustrating the white LED module relating to the fourth embodiment. Fig. 21B is a cross-section of the white LED module taken along a line GG shown in Fig. 21A. Fig. 21C is an enlargement view illustrating a chip-mounted area shown in Fig. 21B.

Fig. 22A illustrates a wiring pattern formed in the white LED module relating to the fourth embodiment. Fig. 22B illustrates a pad pattern formed on a ceramics substrate constituting the white LED module.

Fig. 23A is a perspective view illustrating a lighting apparatus relating to the fourth embodiment. Fig. 23B is a bottom plan view illustrating the lighting apparatus.

Fig. 24 is a perspective exploded view illustrating the lighting apparatus relating to the fourth embodiment.

Fig. 25 shows an emission spectrum of the lighting apparatus relating to the fourth embodiment.

[DESCRIPTION OF CHARACTERS]

0092

2, 102 white LED chip

4 high-resistive Si substrate

6, 106, 206 multilayer epitaxial structure

8, 108, 208 phosphor film

10, 110, 210 p-AlGaN layer

12, 112, 212 InGaN/AlGaN MQW light emitting layer

14, 114, 214 n-AlGaN layer

16 high-reflective electrode

22, 222 depressions

104 n-type SiC substrate

202 white LED array chip

204 AlN substrate

216 p-electrode

[DOCUMENT] Abstract

[SUMMARY]

[AIM] To provide a semiconductor light emitting device which can improve the ratio of accepted finished product, without being increased in size.

[MEANS TO ACHIEVE THE AIM] The semiconductor light emitting device includes: a multilayer epitaxial structure 16 including a light emitting layer12; and a high-resistive Si substrate 4 whose main surfaces are slightly larger than main surfaces of the multilayer epitaxial structure 16. The multilayer epitaxial structure 16 is formed on one of the main surfaces of the high-resistive Si substrate 4 with a space being retained along a periphery of the high-resistive Si substrate 4, and a phosphor film 8 covers side surfaces and a main surface of the multilayer epitaxial structure 16 which is opposite to the main surface to which the high-resistive Si substrate 4 is connected. The multilayer epitaxial structure 16 is first epitaxially grown on a sapphire substrate, and then transferred to the high-resistive Si substrate 4.

[SELECTED FIGURE] FIG.1

Document : Drawings

Fig. 1A

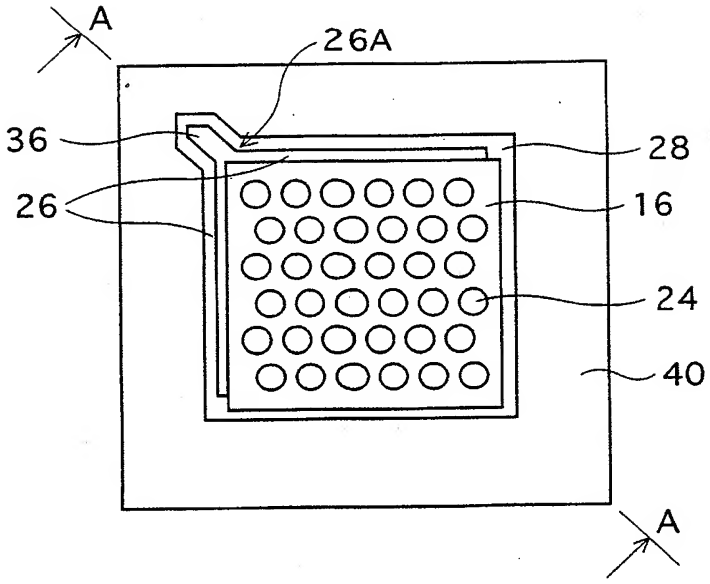


Fig. 1B

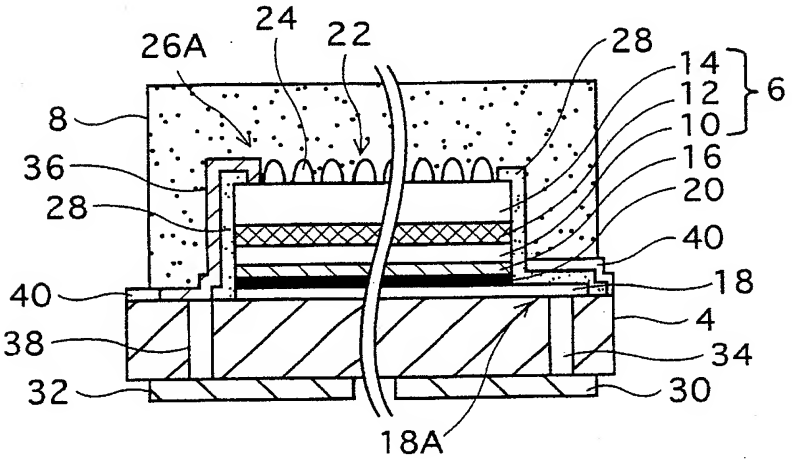


Fig. 1C

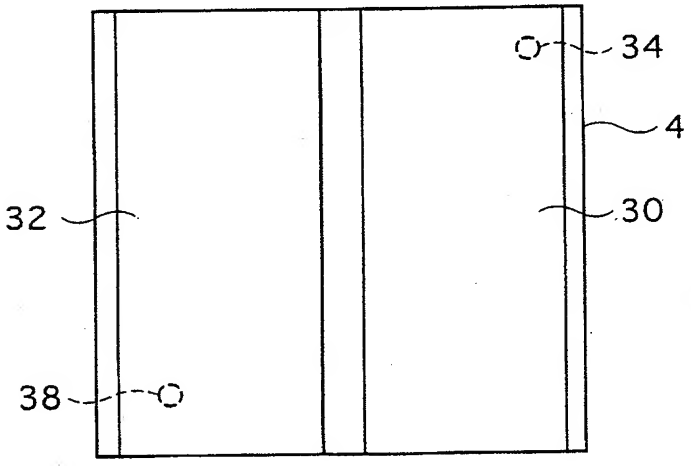
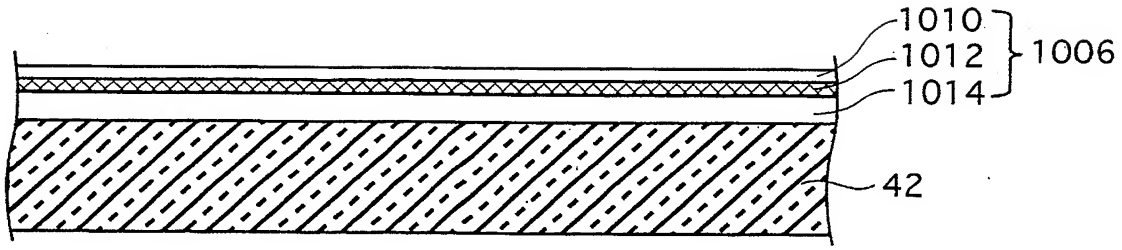
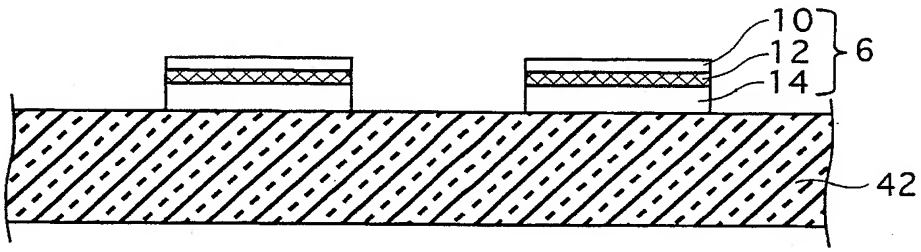


Fig. 2

(A2)



(B2)



(C2)

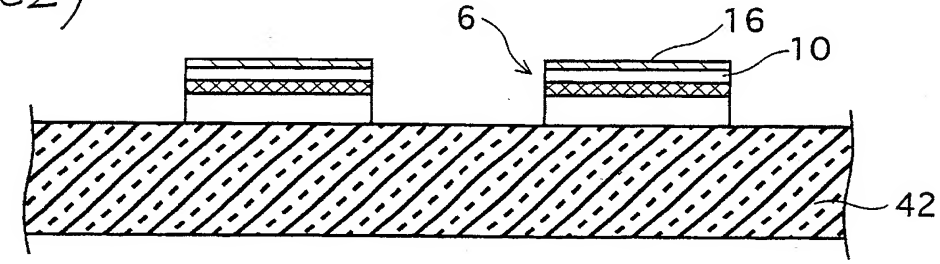
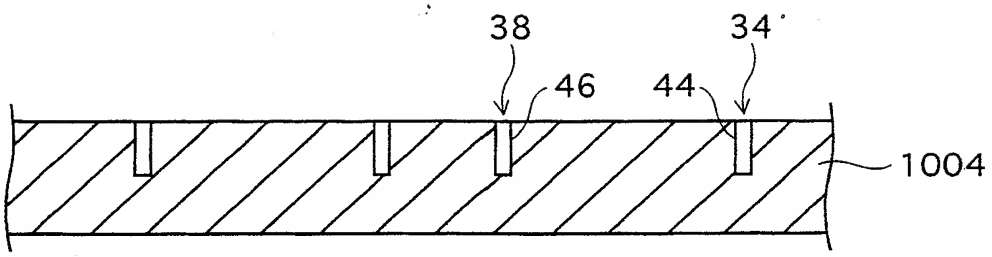
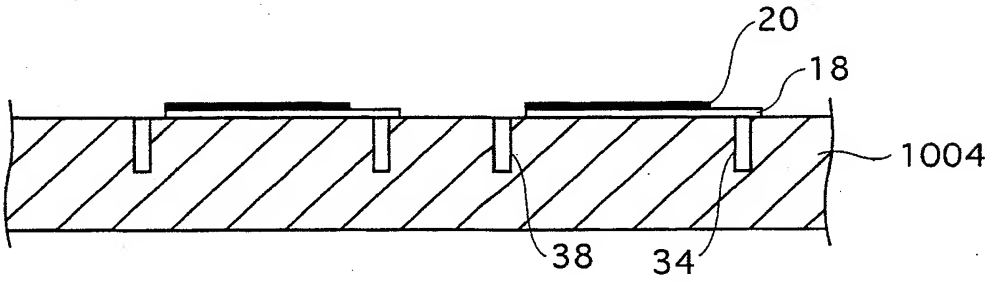


Fig. 3

(D2)



(E2)



(F2)

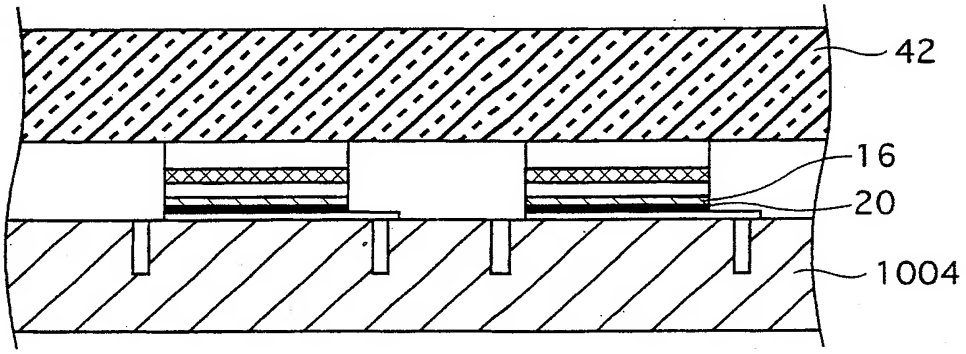
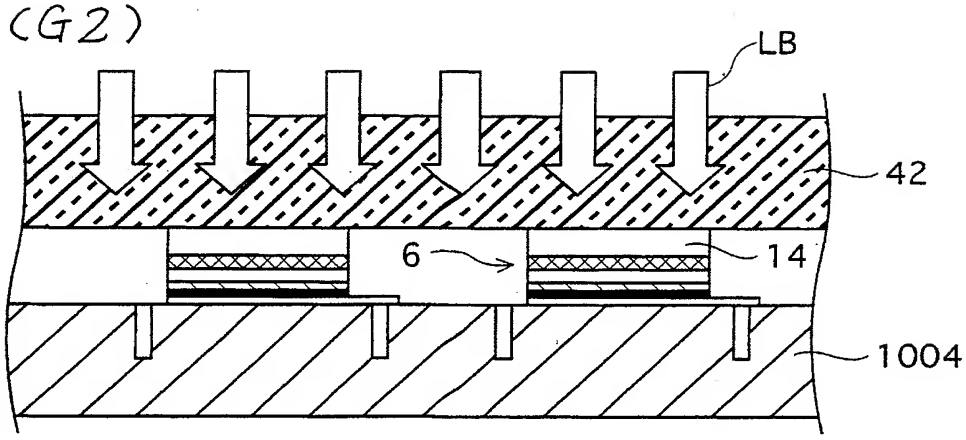
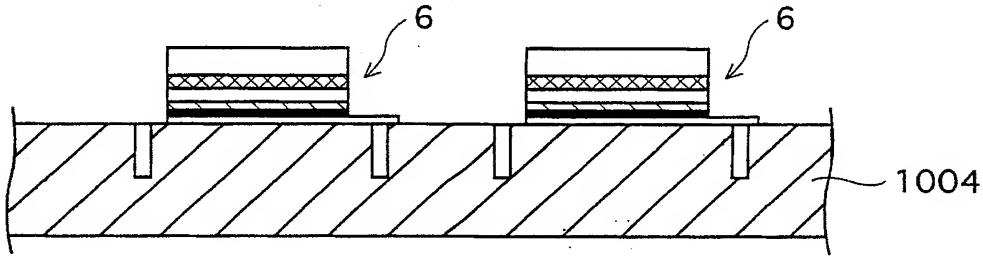


Fig. 4

(G2)



(H2)



(I2)

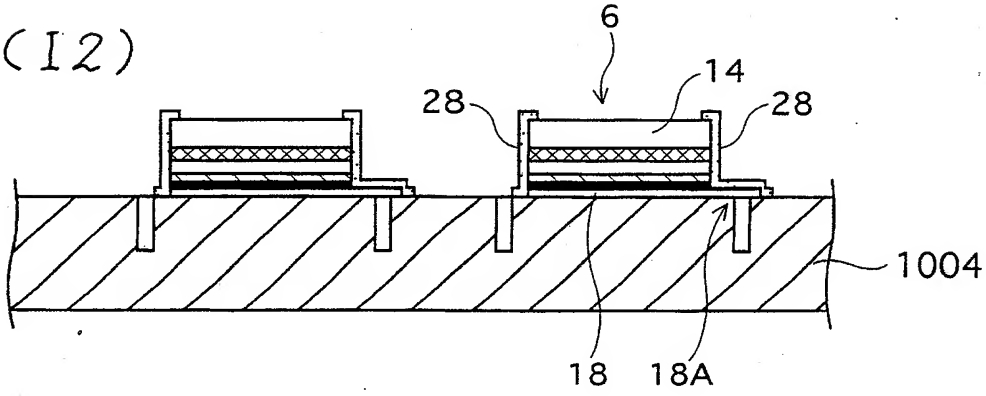
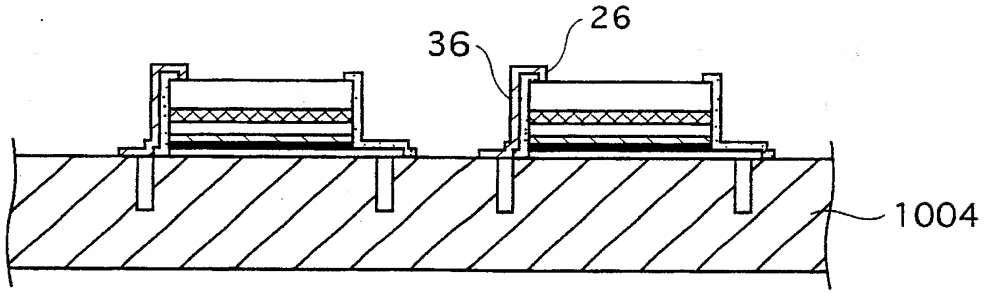
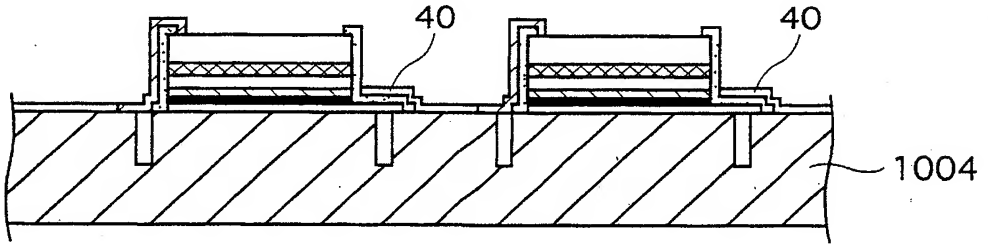


Fig. 5

(J2)



(K2)



(L2)

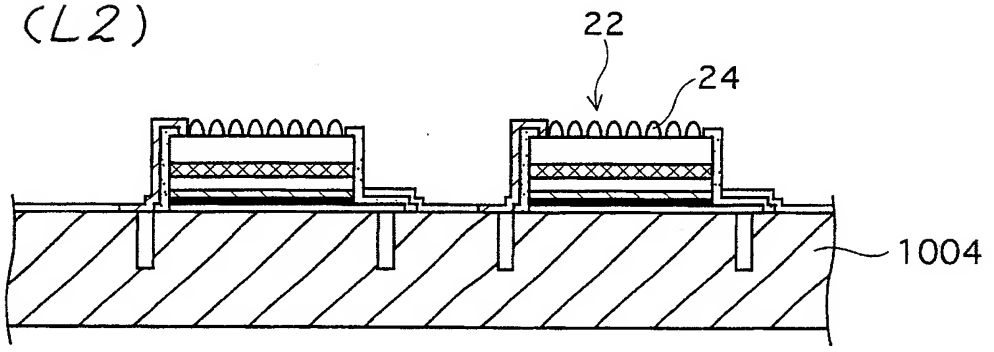
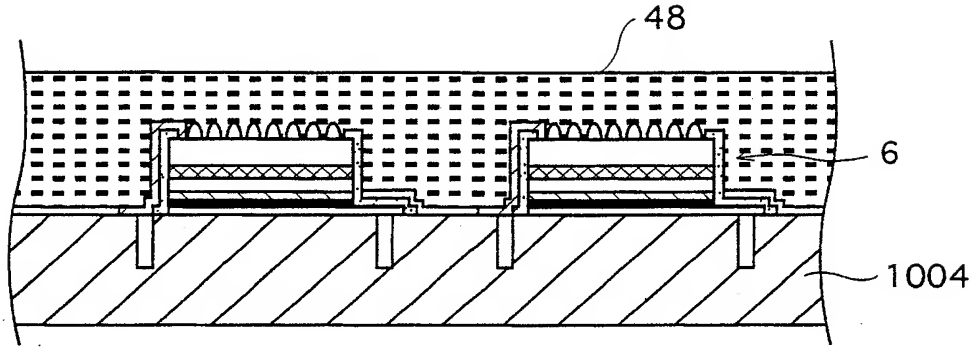
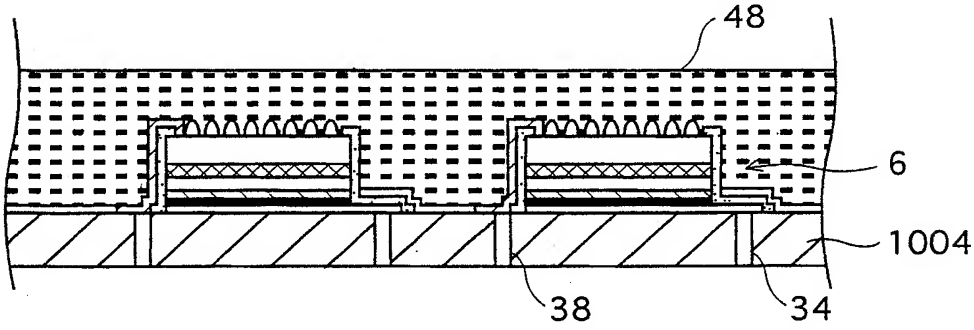


Fig. 6

(M2)



(N2)



(O2)

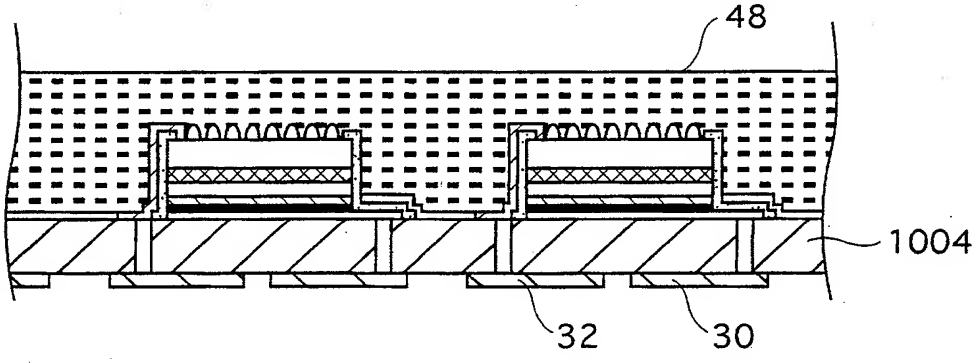
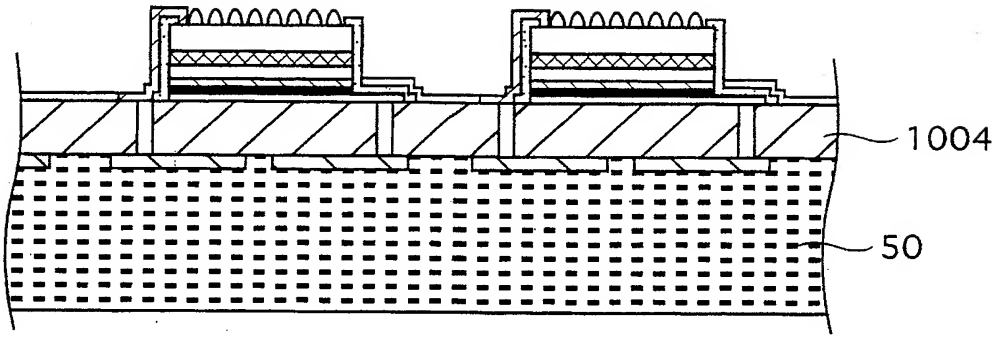
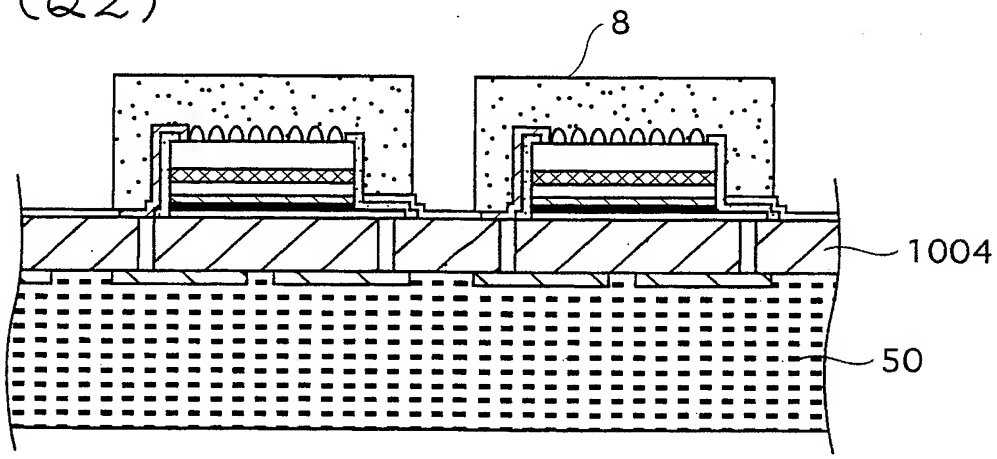


Fig. 7

(P2)



(Q2)



(R2)

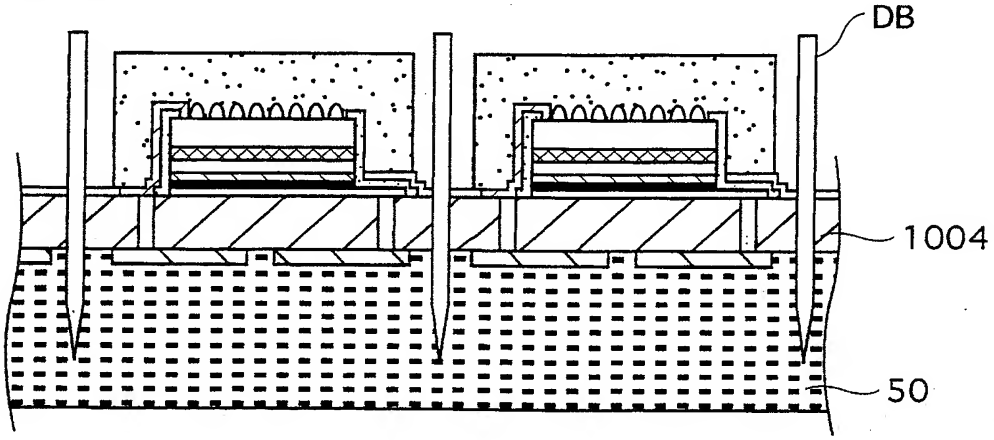


Fig. 8A

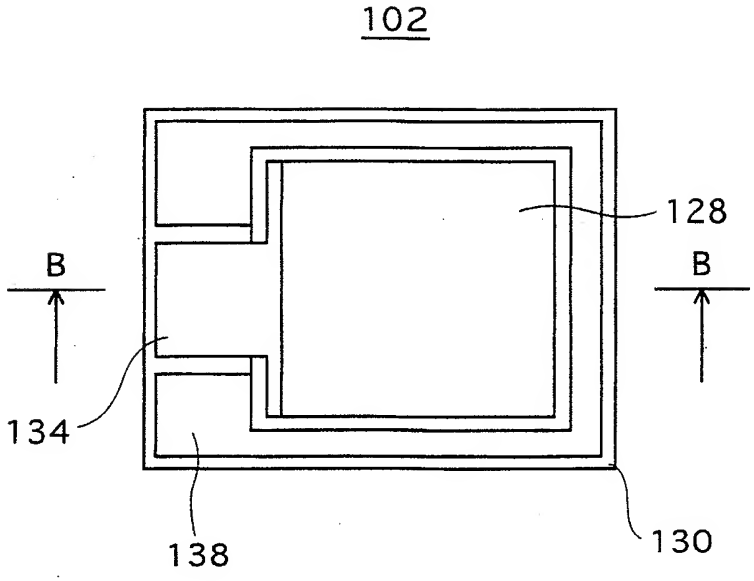

102
128
B
B
134
138
130

Fig. 8B

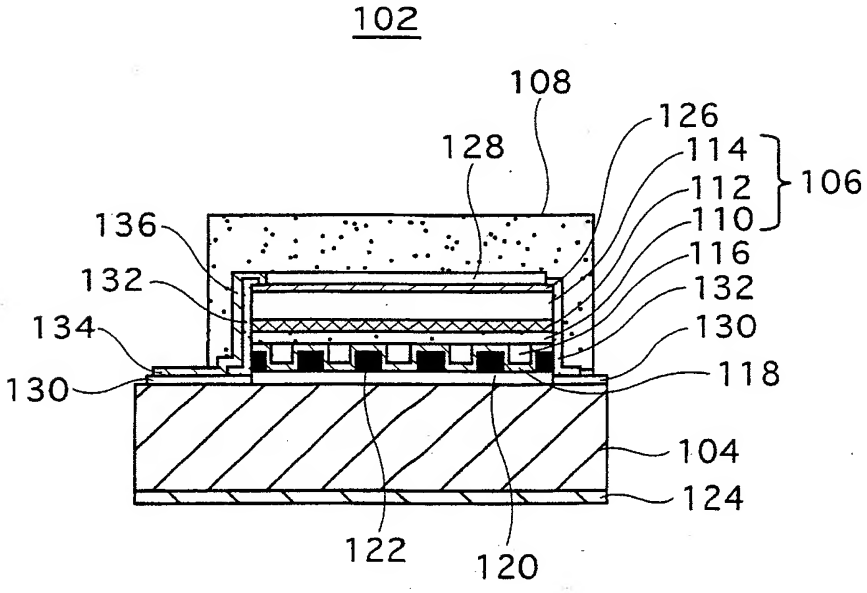
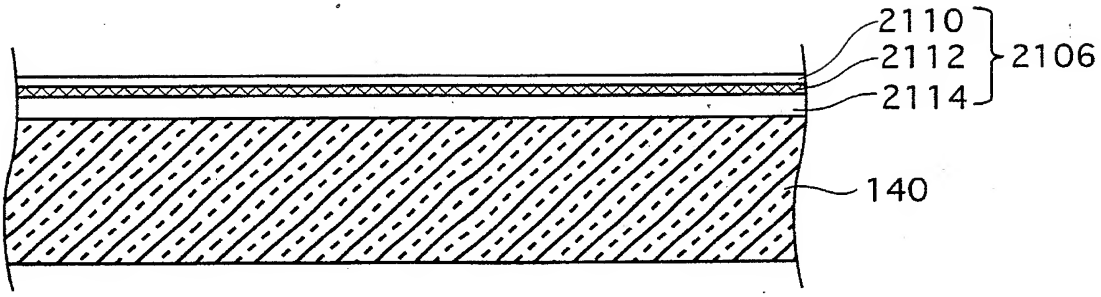
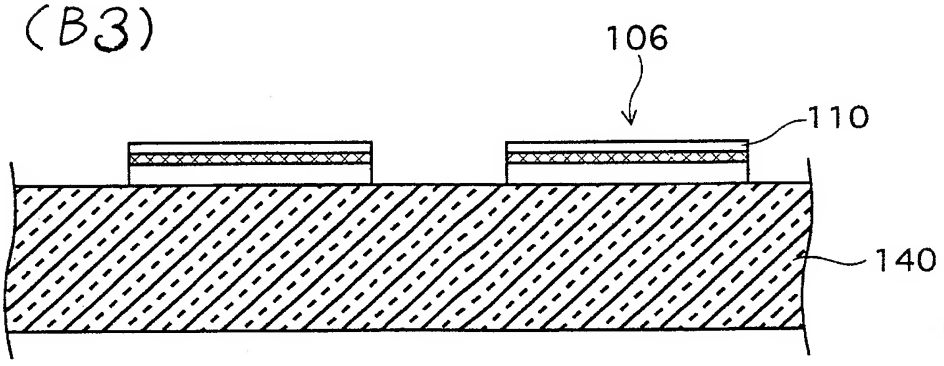

102
108
126
128
114
112
110
106
136
116
132
132
134
130
130
118
104
124
122
120

Fig. 9

(A3)



(B3)



(C3)

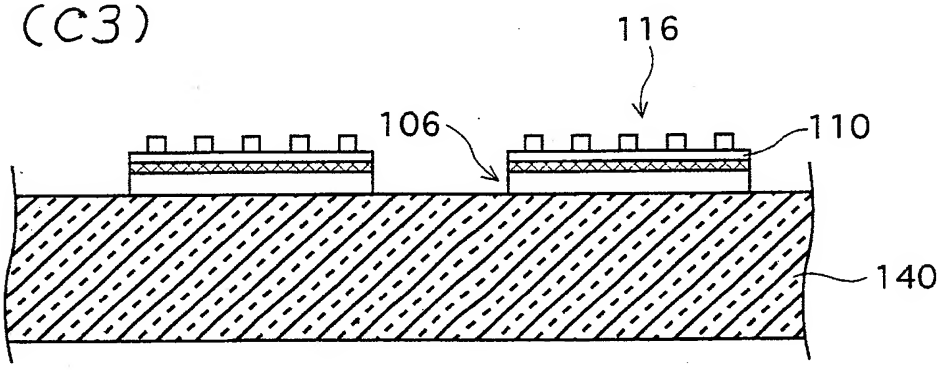
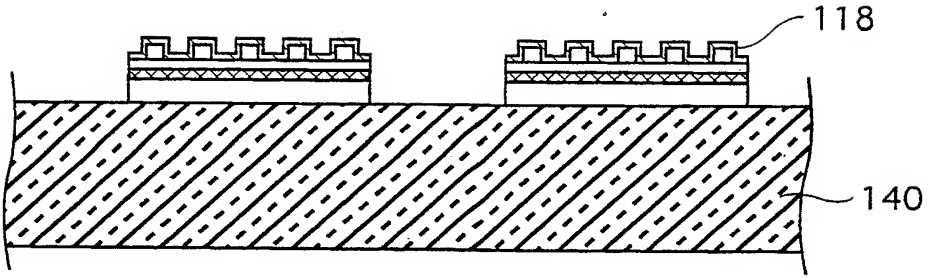
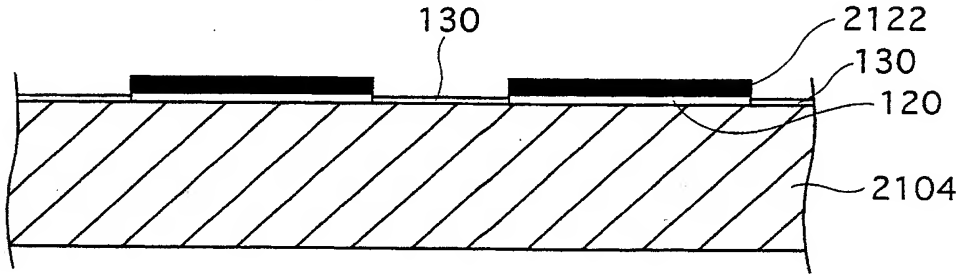


Fig. 10

(D3)



(E3)



(F3)

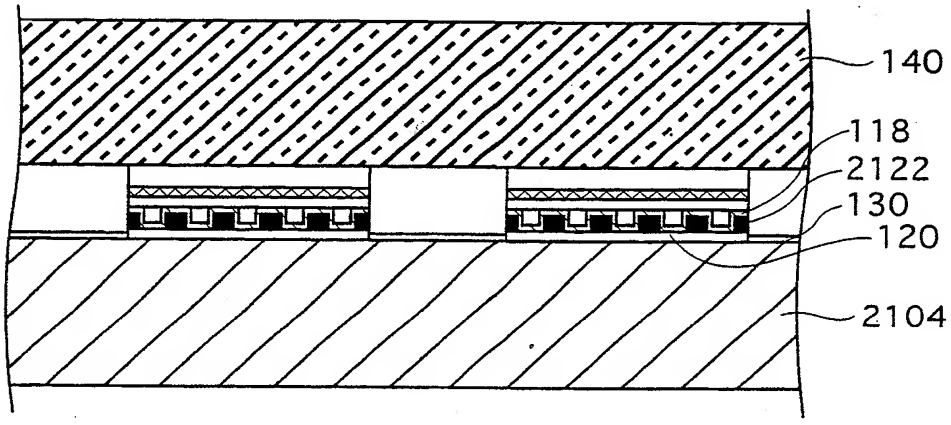
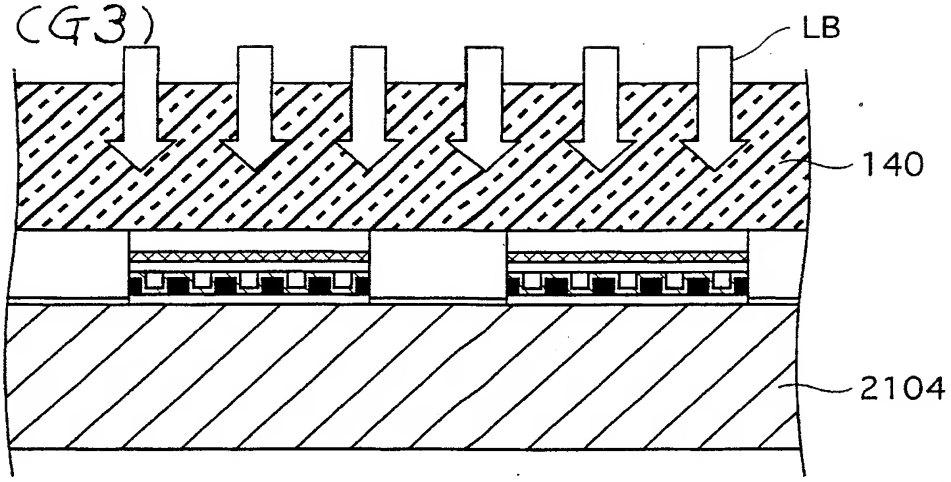
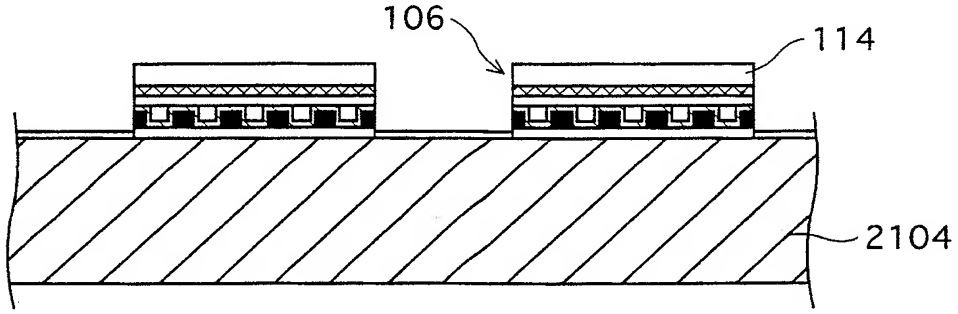


Fig. 11

(G3)



(H3)



(I3)

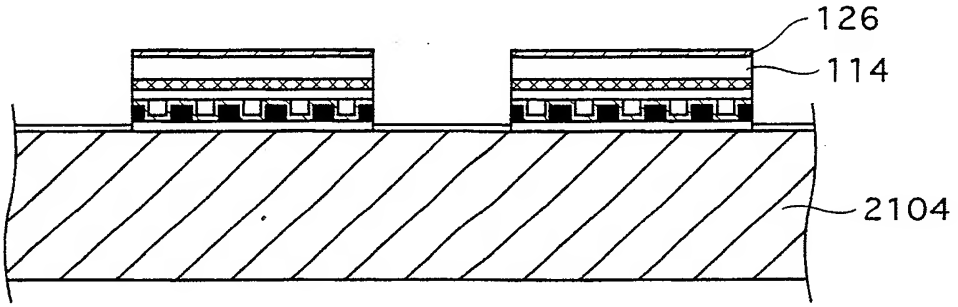
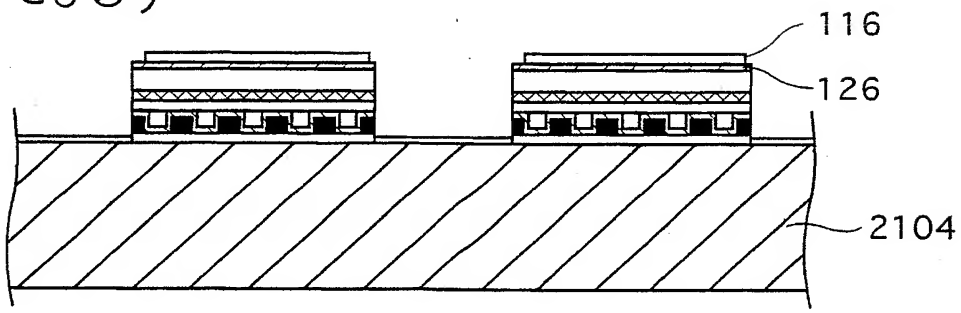
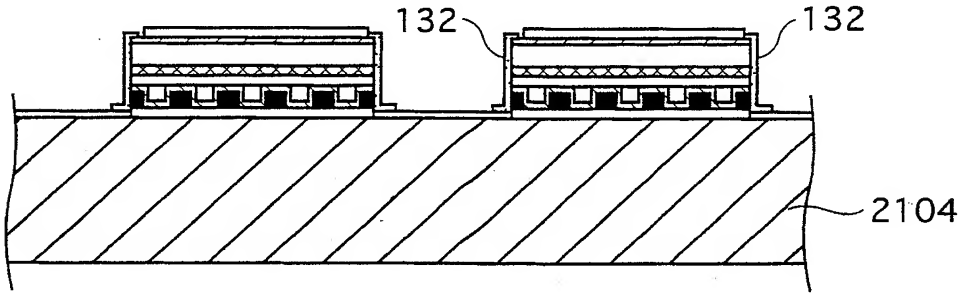


Fig. 12

(J3)



(K3)



(L3)

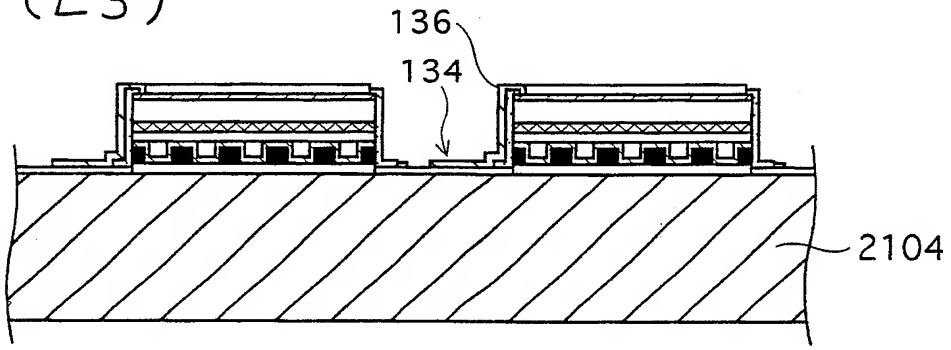
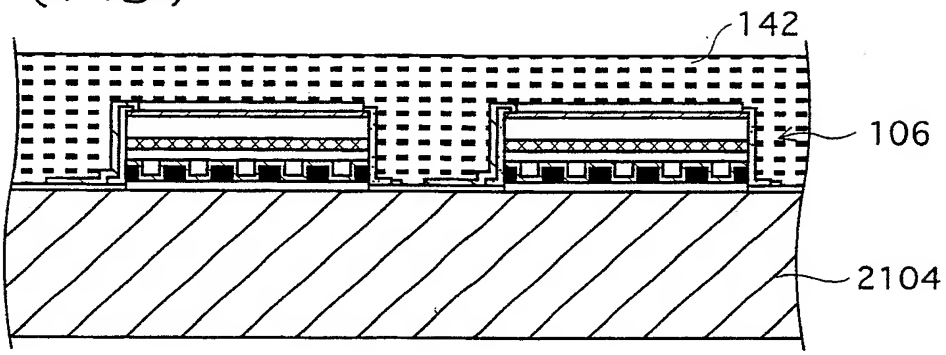
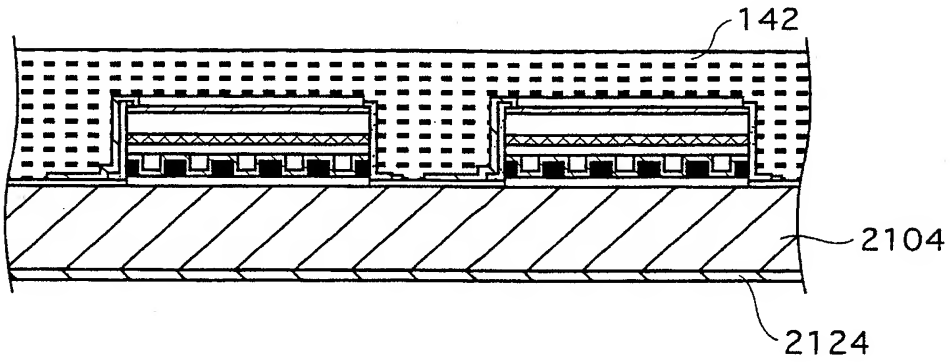


Fig. 13

(M3)



(N3)



(O3)

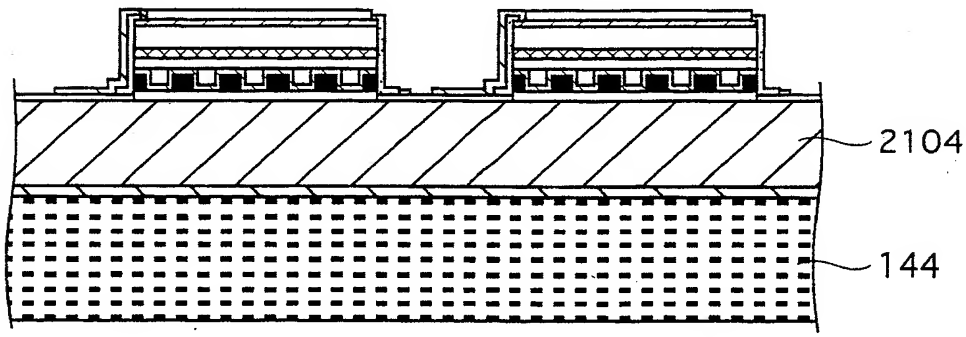
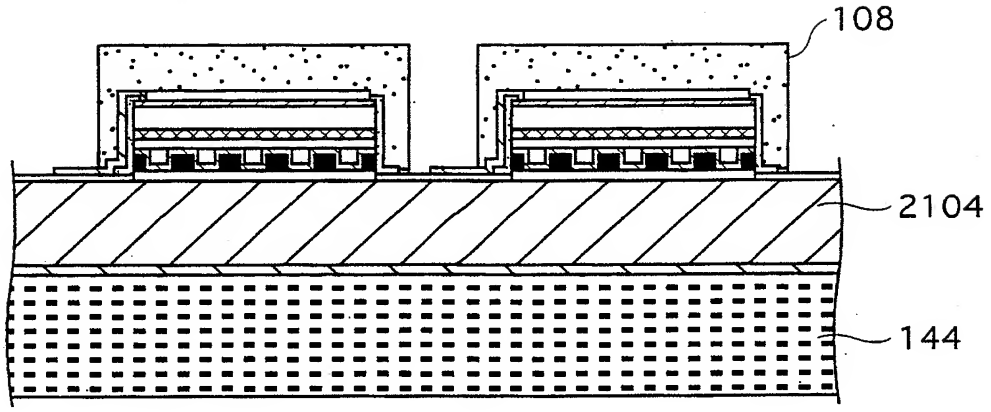


Fig. 14

(P3)



(Q3)

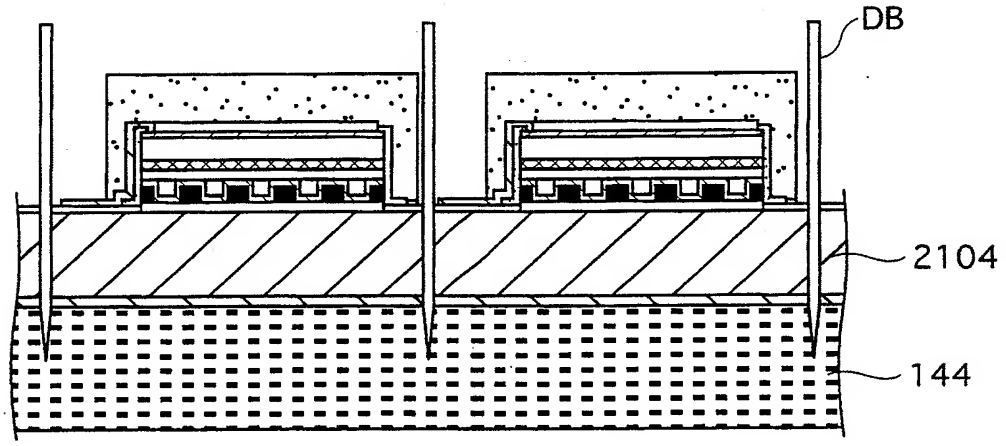


Fig. 15A

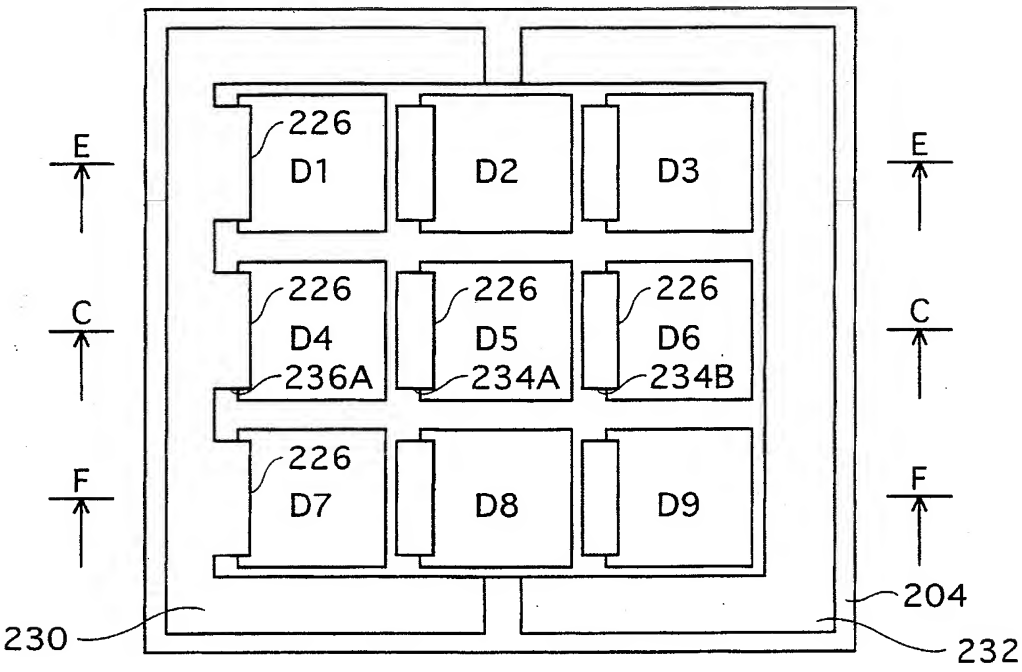


Fig. 15B

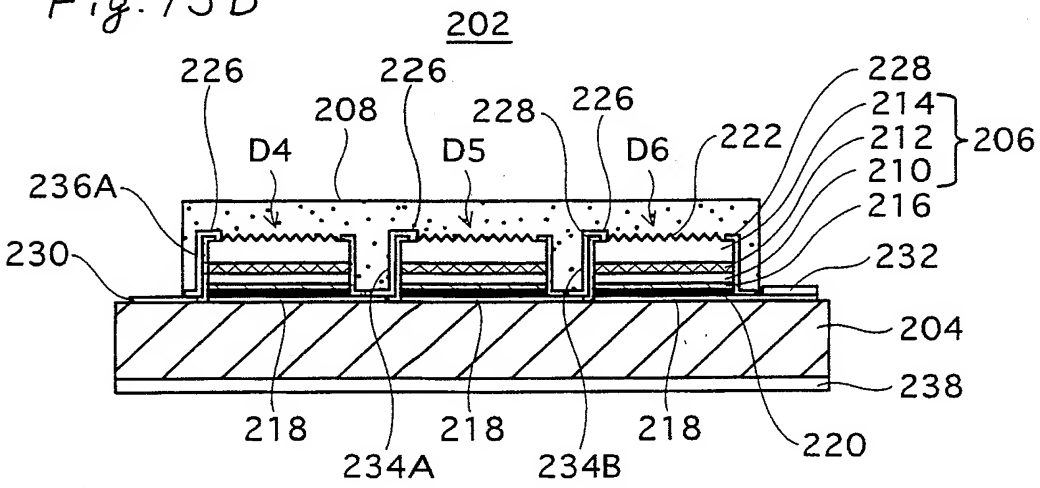


Fig. 15C

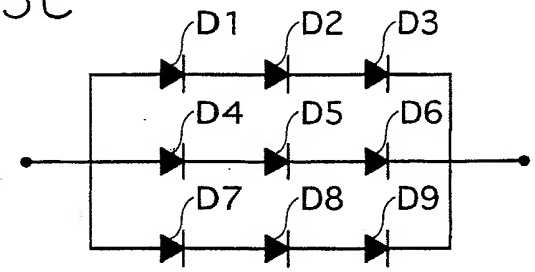
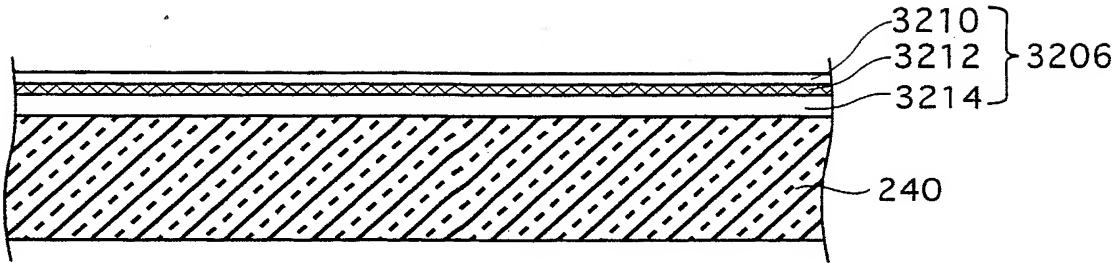
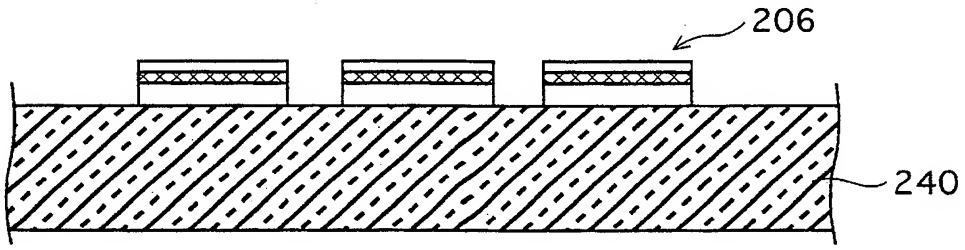


Fig. 16

(A4)



(B4)



(C4)

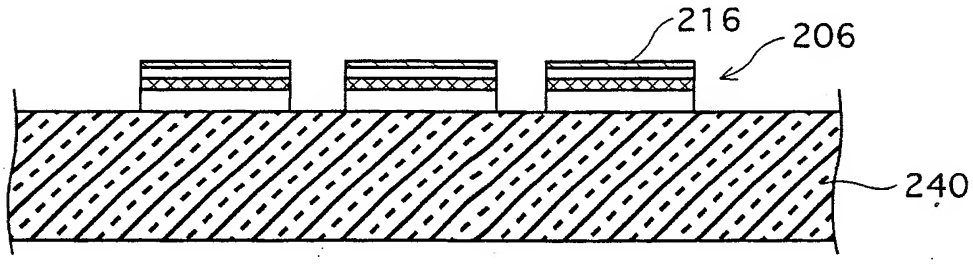
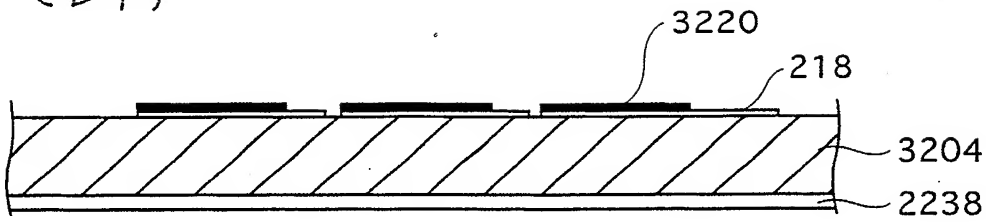
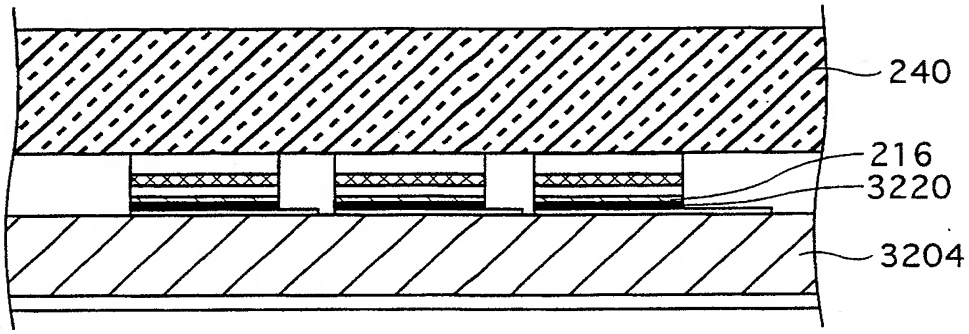


Fig. 17

(D4)



(E4)



(F4)

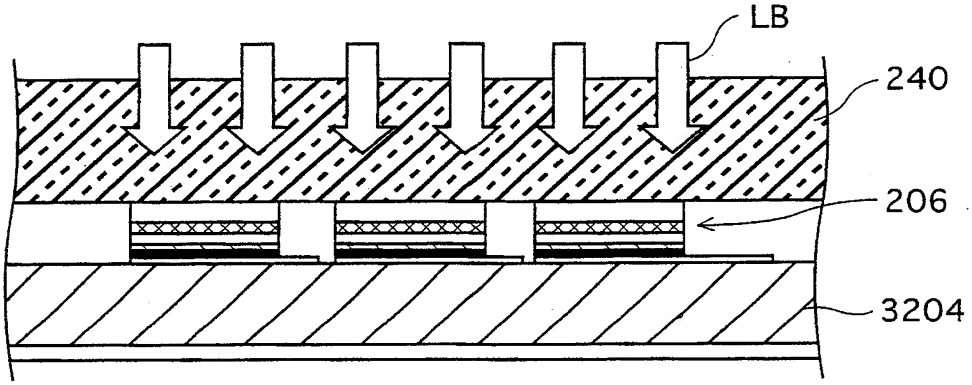
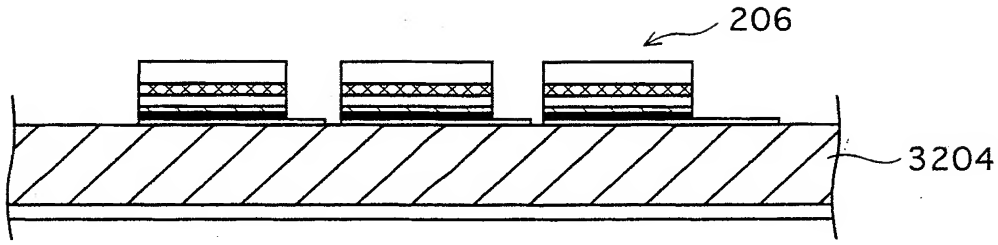
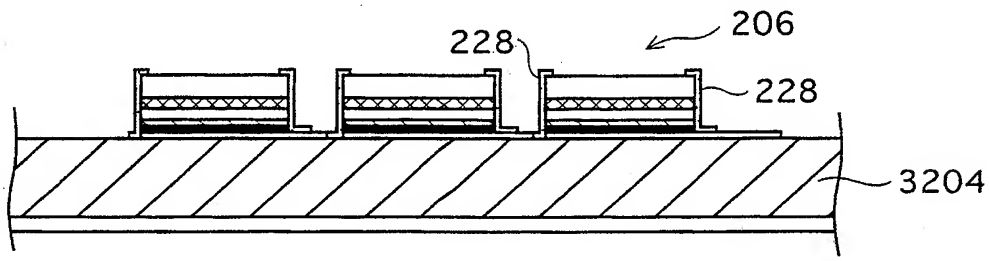


Fig. 18

(G4)



(H4)



(I4)

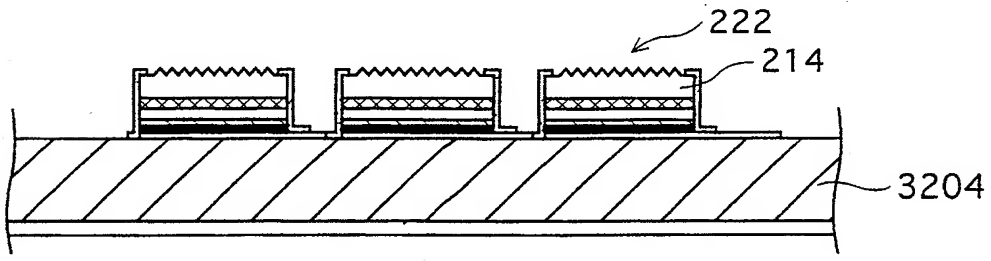
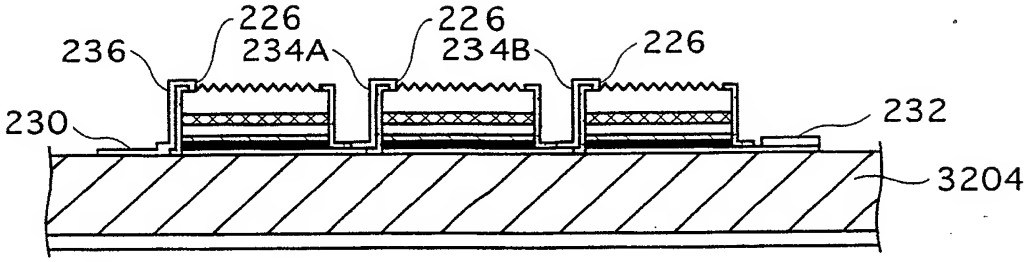
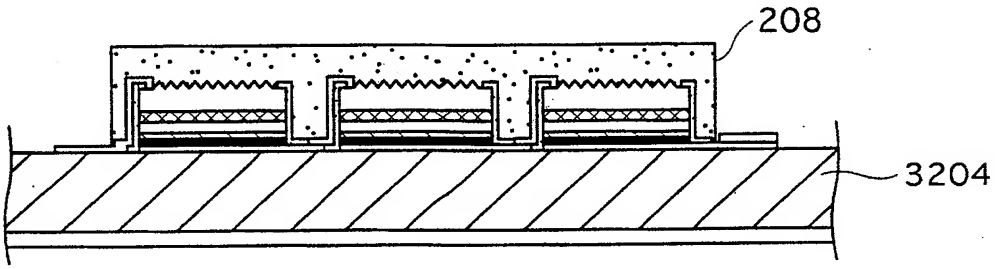


Fig. 19

(J4)



(K4)



(L4)

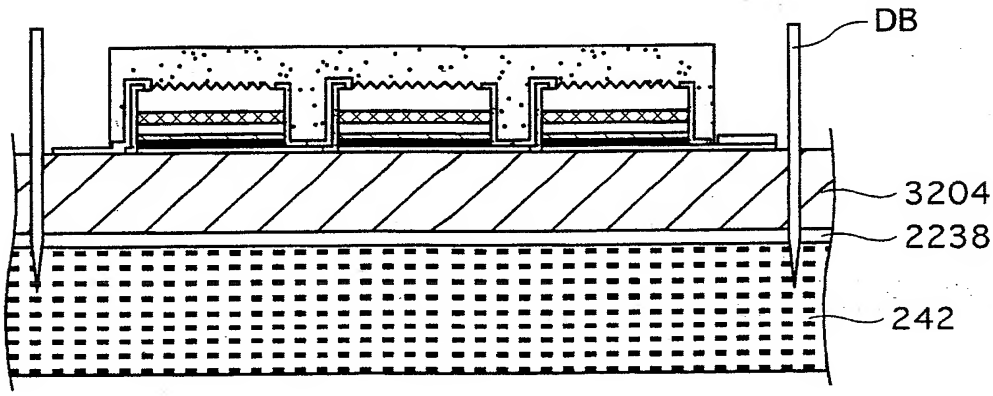


Fig. 20

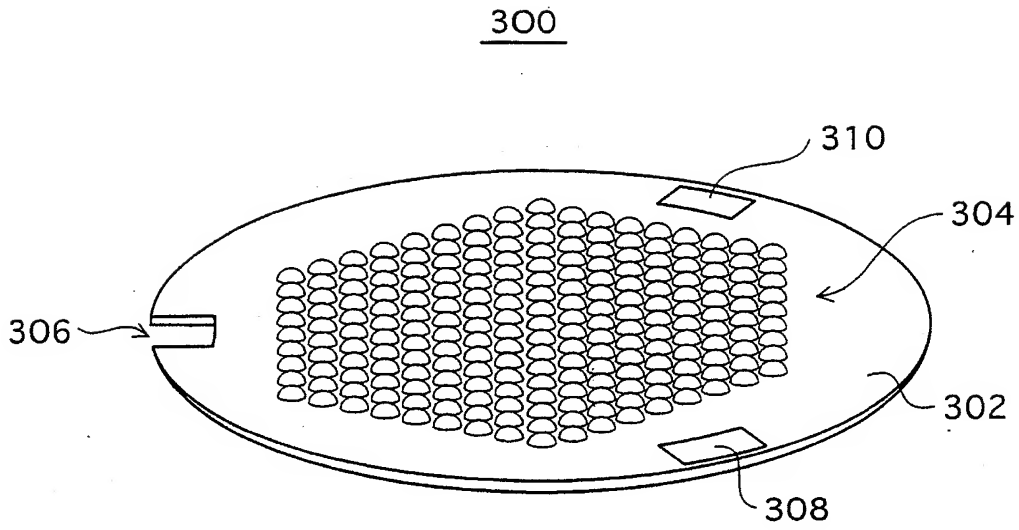


Fig. 21A

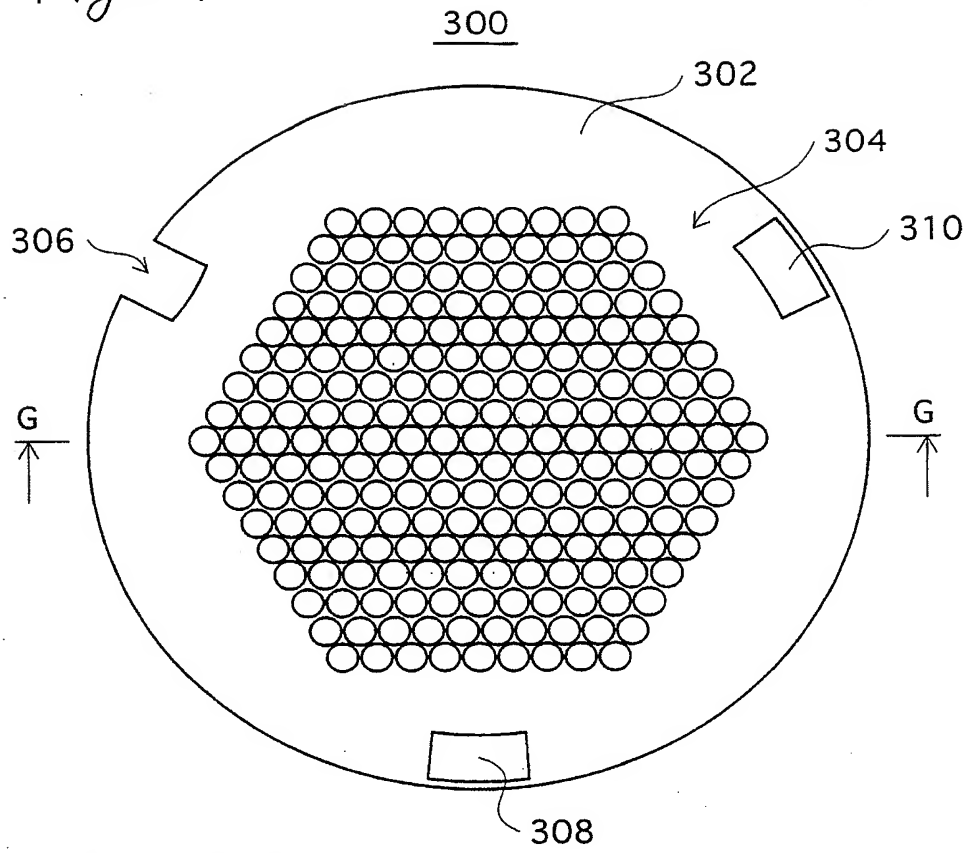


Fig. 21B

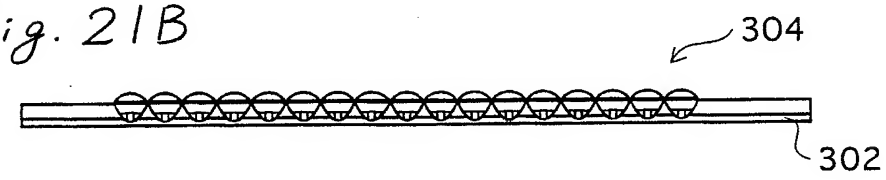


Fig. 21C

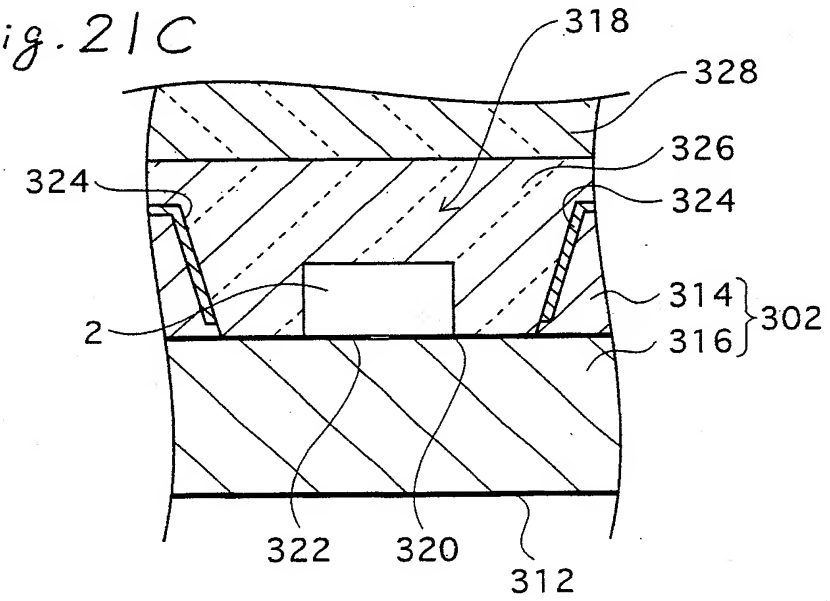


Fig. 22A

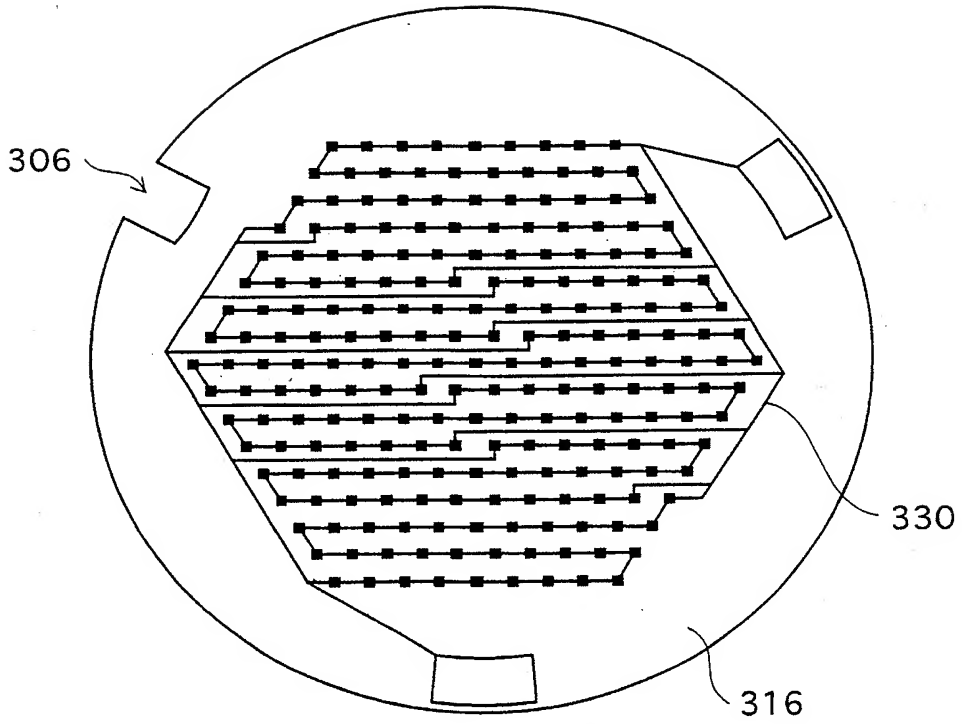


Fig. 22B

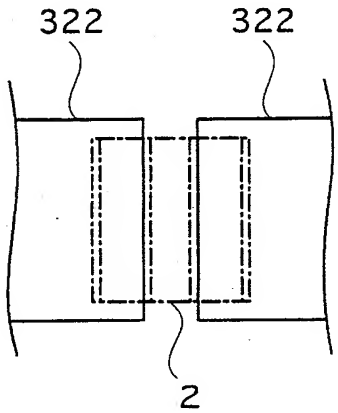


Fig. 23A

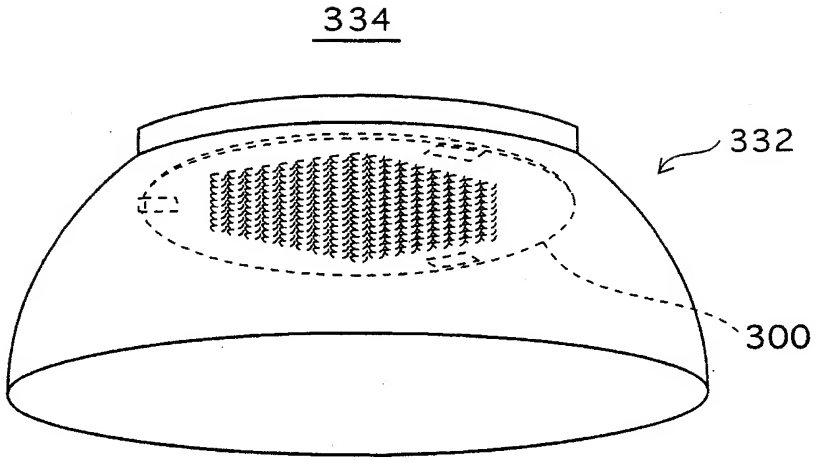


Fig. 23B

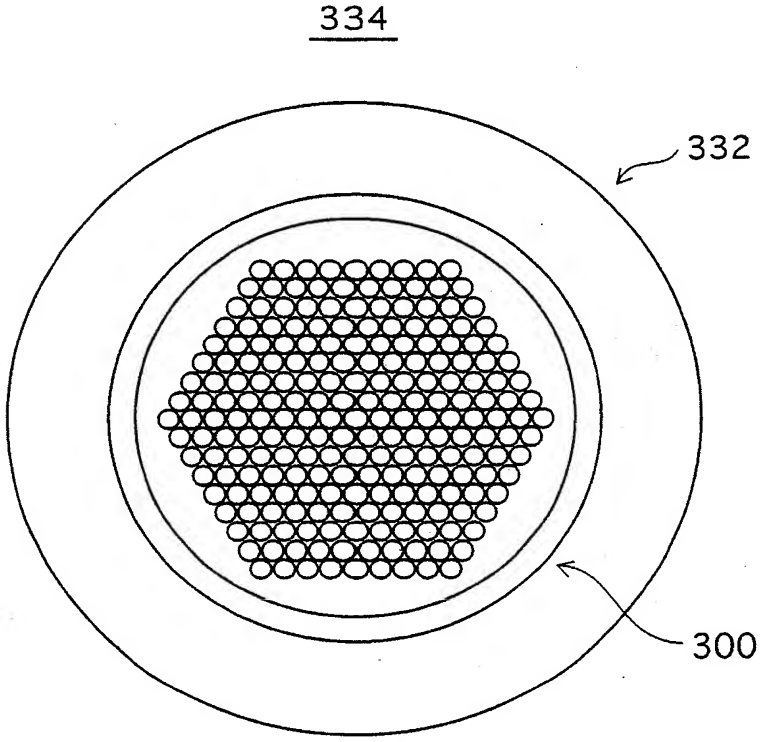


Fig. 24

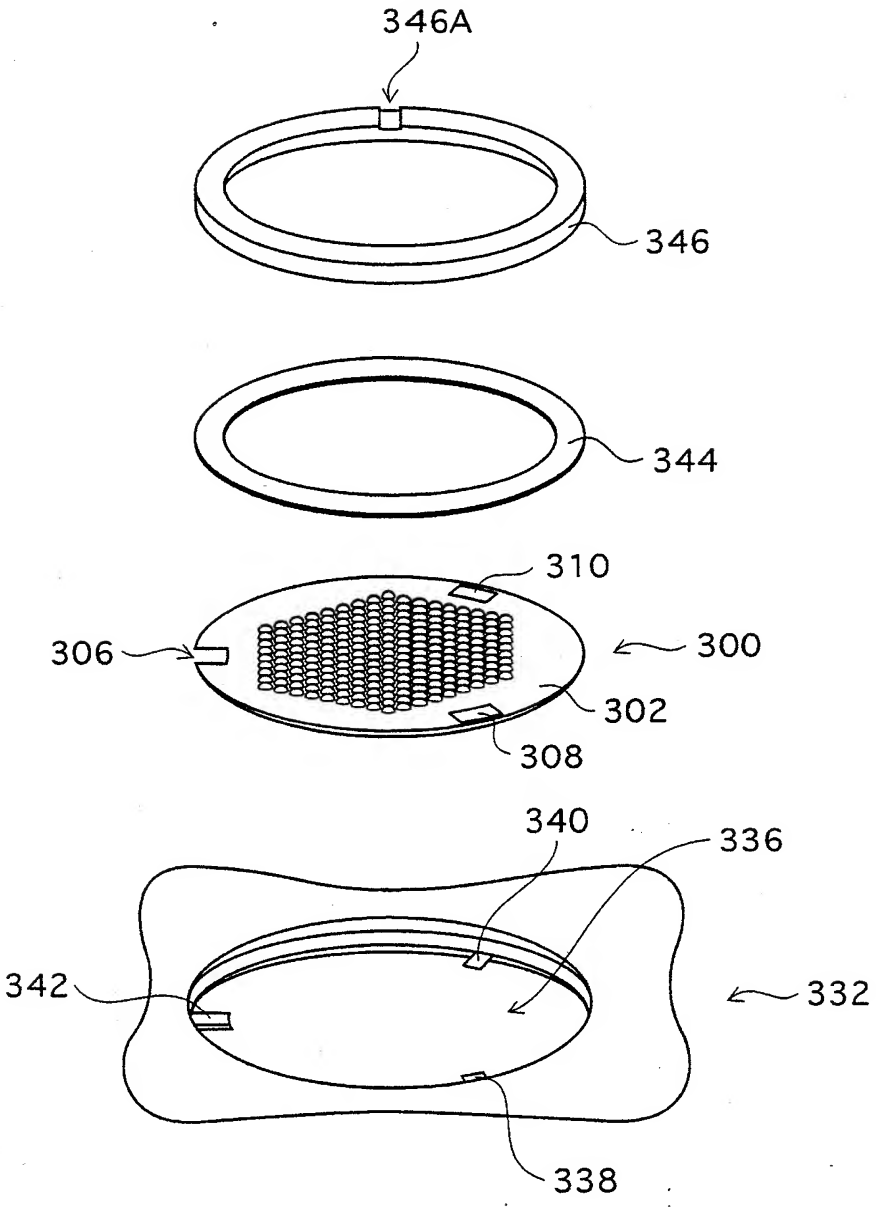
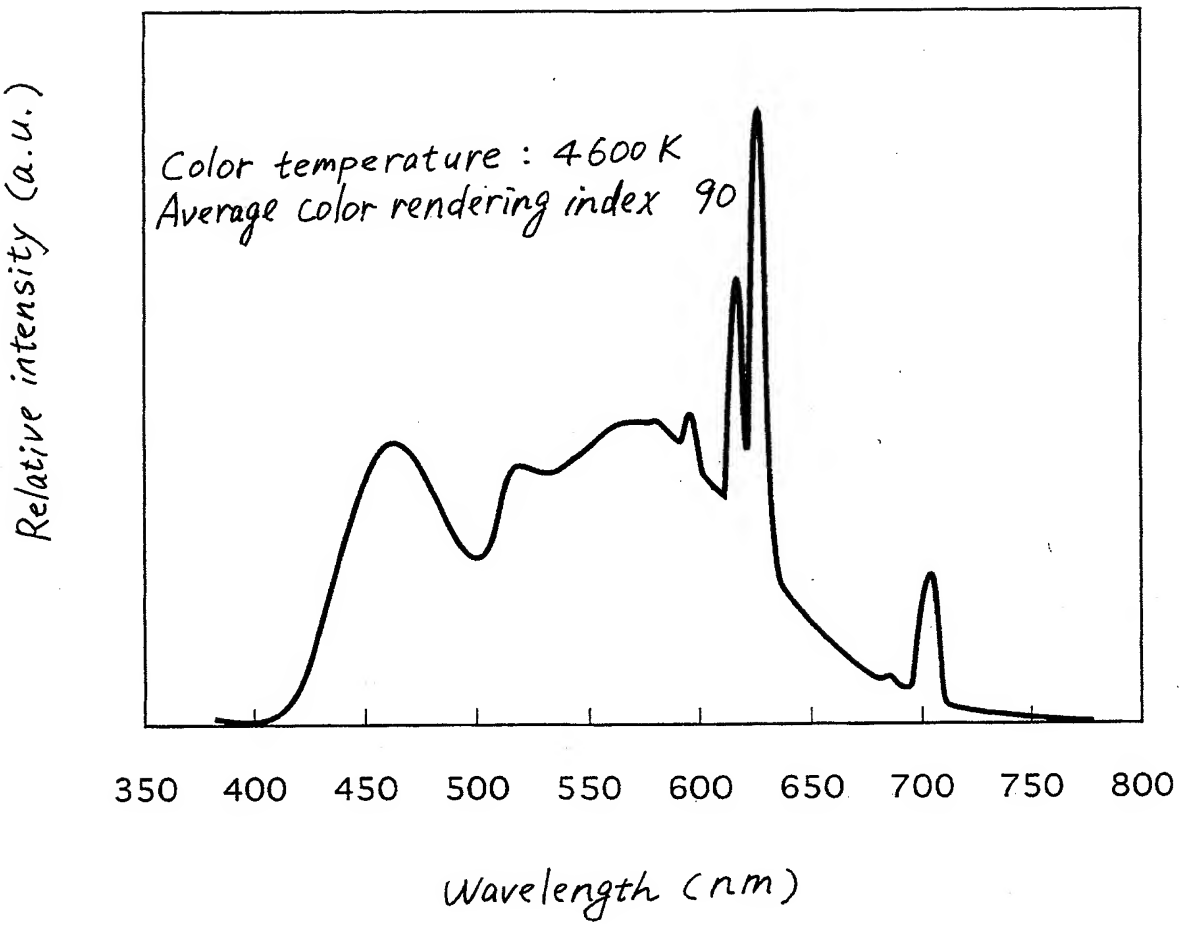


Fig. 25


Color temperature : 4600 K
Average color rendering index 90
Relative intensity (a.u.)
350
400
450
500
550
600
650
700
750
800
Wavelength (nm)